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DESIGN OF A FIBER OPTIC IMAGE TRANSMISSION LINK

THESIS

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An original design is presented for a fiber optic based digital image transmission link operating at a serial bit rate of 250 Mbits/Second. The link is designed as an integral part of an airborne infrared imaging system with particular emphasis on avoiding problems associated with aircraft electromagnetic interference (EMI). Unique features include simplicity (single PC board transmitter and receiver), low power, low cost (under $3,000), and use of the latest off-the-shelf components (including the Gazelle GA9011/GA9012 HOT ROD chip set). Theoretical modeling is used to predict a bit error rate of better than 10^{-15}, while actual measurements include transmission of over 10^{13} bits without any errors (measured bit error rate of at least 10^{-13}). Test results also show that the link is capable of transmitting 640 x 480 pixel (12 bits per pixel) images with no significant image degradation.

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DESIGN OF A FIBER OPTIC IMAGE TRANSMISSION LINK

THESIS

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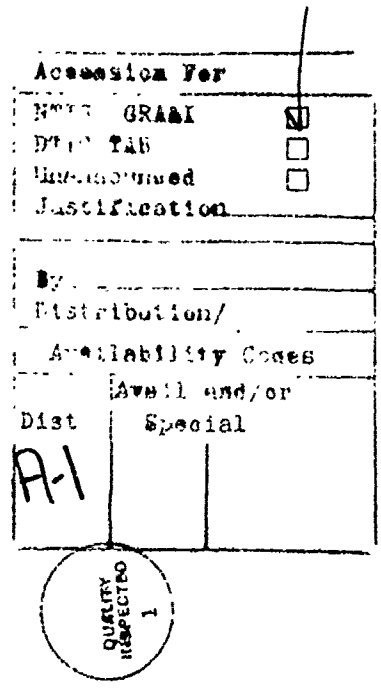

Preface

As in many research projects, the ideas that form the basis for this thesis were born because of a need to solve a problem. The problem was aircraft noise interference in imagery during airborne infrared measurements. The problem existed long before I knew about it, and it was not until I joined the Airborne Measurements Branch of the Air Force Geophysics Laboratory (AFGL) in 1988 that I learned about it and experienced it first hand. Engineers at AFGL had proposed solutions to the problem, but their solutions were not completely practical until new technology in analog-to-digital converters, serial data transmission, and fiber optics became available. The availability of the necessary technology coincided nicely with my assignment to AFGL, and soon I became involved in combining the new technology with the proposed solutions to produce a working system. Research at AFGL eventually led to follow-on work at the Air Force Institute of Technology (AFIT) in the form of this thesis.

I am indebted to many people who have provided the technical and moral support necessary for completion of my thesis. The advice of my thesis committee, including my faculty advisor Lt Col David Norman, and committee members Capt Mark Mehalic and Capt Byron Welsh, has been extremely useful. Also, without the support of my sponsors at AFGL, this thesis would have been impossible. Specific contributors at AFGL include Brian Sandford, John Schummers, John Rex, Sandy Carrow, Paul Millard, and Capt Herb Klopfenstein. Particular thanks are in order for Sandy Carrow, who's long hours of work in laying out and building the PC boards made it possible to turn the design into real hardware.

Words cannot describe the extent of the gratitude I feel for the sacrifices made by my wife, Anna, and my three beautiful daughters Sarah, Rebecca, and Katherine (who's birth during final exam week provided extra excitement). I must also mention

the tremendous support provided by my Mother, Myrna Redd, and my Father, Frank Redd (a great enineer and inspiration) over a period of many years.

Justin David Redd

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Abstract

An original design is presented for a fiber optic based digital image transmission link operating at a serial bit rate of 250 Mbits/Second. The link is designed as an integral part of an airborne infrared imaging system with particular emphasis on avoiding problems associated with aircraft electromagnetic interference (EMI). Unique features include simplicity (single PC board transmitter and receiver), low power, low cost (under $3,000), and use of the latest off-the-shelf components (including the Gazelle GA9011/GA9012 HOT ROD chip set). Theoretical modeling is used to predict a bit error rate of better than 10^{-15}, while actual measurements include transmission of over 10^{13} bits without any errors (measured bit error rate of at least 10^{-13}). Test results also show that the link is capable of transmitting 640 x 480 pixel (12 bits per pixel) images with no significant image degradation.

10 to the minus 13th power

10 to the minus 15th power

10 to 13th power

DESIGN OF A FIBER OPTIC IMAGE TRANSMISSION LINK

I. Introduction

1.1 General Background

This thesis project is a result of the continuing development of Platinum Silicide (PtSi) Focal Plane Array (FPA) Infrared (IR) cameras. PtSi FPA cameras record images in the 3 to 5 μm region of the infrared spectrum. The basic technology for the PtSi FPA IR camera was developed under the direction of the Rome Laboratory (RL) at Hanscom AFB, Massachusetts. In 1985, the Geophysics Directorate of the Phillips Laboratory (PL/GD), also at Hanscom AFB, became interested in using PtSi technology aboard aircraft and began a joint project with RL to develop cameras for use in airborne applications. The resulting 160 x 244 pixel element PtSi camera system proved to be a valuable instrument. PL/GD has made many modifications to the original camera design in order to improve performance and has initiated plans for additional modifications.

PL/GD is currently interested in exploiting the latest advances in PtSi IR camera technology by developing a flight qualified 640 x 480 pixel element PtSi camera. Accomplishing this task will require modifications to existing systems as well as development of new technologies. One critical problem area in this effort involves determining a method to transmit raw image data from a moveable, window-mounted camera to a rack-mounted image processor within an electrically noisy aircraft environment. This thesis presents one possible solution to that problem.

1.2 Problem Statement

The Geophysics Directorate of the Phillips Laboratory (PL/GD) needs a method to transmit 640 x 480 pixel infrared images through an electrically noisy aircraft environment while maintaining image quality.

1.3 Research Objectives

The objectives of this thesis are to: 1) present an original design for a fiber optic image transmission link capable of transmitting 640 x 480 pixel images, 2) establish criteria for determining the success or failure of the image transmission link, 3) mathematically model the design to predict its performance, and 4) verify theoretical predictions through actual measurements.

1.4 Summary of Current Knowledge

Published material dealing with dedicated fiber optic image transmission as an integral part of a camera system is virtually non-existent. This lack of directly applicable research can be attributed in part to the fact that past fiber optics research has focused on exploiting the high bandwidth and low attenuation properties of optical fiber, while this project seeks instead to exploit the insensitivity of fiber optics to electromagnetic interference. Also, until recent advances in small, low power, analog-to-digital (A/D) converters, parallel-to-serial data encoding devices, and fiber optic components, design of a fiber optic image transmission link as an integral part of an infrared camera system was impractical. These recent advances have made it possible for the first time to explore the integration of a fiber optic link directly into the camera system.

This thesis builds on ideas and research accomplished at the Geophysics Directorate of the Phillips Laboratory at Hanscom AFB, Massachusetts in 1989 and 1990. The events leading up to this thesis are the subject of Chapter II.

1.5 Assumptions

At present, the 640 x 480 pixel PtSi camera is still in the design stage and exact data on signal format is unavailable. For purposes of this thesis, it is assumed that the signal format will be similar to that of the existing PL/GD 160 x 244 PtSi camera. Under this assumption, input circuit design for the fiber optic image transmission link generally follows designs used previously in data link testing with the 160 x 244 PtSi camera [18].

An important part of this thesis is determination of bit error rate (BER) performance levels necessary to transmit images with no significant degradation (Chapter

IV addresses the definition of "significant" image degradation). Mathematical modeling and calculation of the necessary BER is based on the best possible signal to noise ratio (SNR) at the output of the IR camera. SNR data does not exist on the 640 x 480 camera, but data has been published on the 160 x 244 camera [14, 15, 16]. It is assumed that the 640 x 480 camera will have a best possible SNR similar to the 160 x 244 camera. This assumption is based on measurements and models documented in the sources cited previously in this paragraph and its validity is addressed in more detail in Chapter IV.

1.6 Scope and Limitations

This thesis does not attempt to compare the fiber optic image transmission link with other possible image transmission techniques. At present, a suitable method of transmitting infrared images in the context of the thesis problem has not been devised. This thesis concentrates only on devising an acceptable one. This thesis does not attempt to determine the relative performance of one design solution versus another. It does establish an absolute measure of the performance of the fiber optic image transmission link which may be useful in comparisons with possible future design solutions.

This thesis does not evaluate the performance of the fiber optic image transmission link in an actual aircraft setting. Evaluation was accomplished in a laboratory environment with no attempt to simulate aircraft conditions. It is recognized that many designs which perform flawlessly in the laboratory fail miserably aboard aircraft. Flight testing is beyond the scope of this thesis, however.

1.7 General Approach

To successfully complete this thesis, four general areas of effort (corresponding to the research objectives listed in Section 1.3) were necessary: hardware design, determination of success criteria, theoretical performance predictions, and hardware construction/testing. The order in which these areas of effort are presented reflects the limited flexibility in methods of hardware design. Because of limited choices in the area of components that meet the size, speed, and power requirements of the image transmission link, hardware design was accomplished first. Once the tentative hardware design was complete, the design was evaluated (determination of success

criteria, theoretical performance predictions) and finally, after the design was proven theoretically, the hardware was constructed and tested.

1.7.1 Hardware Design Hardware design of the fiber optic image transmission link (the subject of Chapter III) centers around the newly introduced GA9011 and GA9012 (HOT ROD^{TM}) gallium arsenide chip set built by Gazelle Microcircuits, Inc. The GA9011 HOT ROD transmitter accepts 40–bit parallel digital input words and converts them to 50–bit serial data blocks. The GA9012 HOT ROD receiver receives the 50–bit serial data blocks and converts them back to the original 40–bit parallel digital words. The HOT ROD chip set is capable of operation at serial data rates of up to 10^9 bits per second.

The fiber optic image transmission link is physically composed of two separate printed circuit boards (a transmitter board and a receiver board) connected via a fiber optic cable. The input to the transmitter consists of a 50 ohm coaxial cable which carries the raw analog data signal from the PtSi camera. The input analog data signal is sampled at the pixel rate of 10 MHz and converted to 12–bit pixel words. The pixel words are then combined, in groups of three, to form a 36–bit parallel data word for input to the HOT ROD transmitter. The HOT ROD transmitter converts the 36–bit parallel input to a serial 250 Mbit/second data stream which drives a fiber optic transmitter. The fiber optic transmitter converts the signal to optical pulses which are coupled into a fiber optic cable. At the other end of the cable, a fiber optic receiver converts the optical pulses to a serial bit stream which is sent to the HOT ROD receiver. The HOT ROD receiver converts the serial data to 40–bit parallel data words which are broken up into the three original 12–bit pixel words and formatted for output to the image processor.

1.7.2 Determination of Success Criteria Success of the fiber optic image transmission link is defined in terms of the amount of degradation suffered by the image data during the transmission process relative to the noise inherent in the image prior to transmission. The subject of what constitutes success addressed in detail in Chapter IV. Two levels of success are defined: absolute success and practical success. Absolute success occurs when the probability of any particular pixel error magnitude due to noise introduced by the image transmission link is less than 1% of the probability of that same pixel error magnitude due to noise introduced prior to transmission over the full range of possible pixel error magnitudes. Since absolute

success is overly restrictive, the definition of practical success is based on the manner in which the images are processed and used (see Chapter IV). Practical success is achieved when pixel errors due to the image transmission link occur less than once every other frame.

1.7.3 Theoretical Performance Predictions Theoretical modeling of the fiber optic image transmission link is the subject of Chapter V, which includes analysis of such error mechanisms as analog–to–digital conversion error, high–speed CMOS circuitry error, optical detection error, and decoding error. Optical detection and decoding error are shown to be dominant. Standard noise models are used to calculate expected probability of bit error between the fiber optic transmitter and receiver. This expected probability of bit error is then compared to the link success criteria to demonstrate that the link is theoretically capable of successful operation.

1.7.4 Hardware Construction/Testing Hardware testing was accomplished using a custom test arrangement (see Chapter VI). A sequence generating circuit was used to generate a sequence of 12–bit simulated pixel words. The 12–bit A/D converter was removed from the ITL transmitter and the simulated pixel words were used as the input to the transmitter in place of the A/D converter output. The data strobe of the ITL receiver was used to drive an sequence generator identical to the one used at the transmitter. The received data was then compared to the output of the sequence generator. Bit errors produced comparison differences that were used to generate error signals which were counted over a period of time to determine the average bit error rate.

1.8 Benefits of the Research

PtSi FPA cameras have proven to be extremely useful. Research in progress, along with recent advances, promises to move this technology into an increasingly important role in the field of infrared imaging. The fiber optic image transmission link solves an important problem in the effort to incorporate PtSi FPA cameras into the aircraft environment.

1.9 Thesis Overview

Following this introductory chapter are four additional chapters. Chapter II provides a more detailed historical background of PtSi FPA cameras and the re-

search that led up to this thesis. Chapter III covers the hardware design. Chapter IV lays out the detailed approach used to determine the success criteria and define significant image degradation. In Chapter V, theoretical predictions of ITL performance are formulated, and in Chapter VI, actual performance measurements are documented and compared to the theory. Finally, Chapter VII provides conclusions and recommendations.

II. Historical Background

2.1 Introduction

As noted in Section 1.4, published background material that is applicable to this thesis is vitually non–existent. For that reason, the traditional *Literature Review* chapter is not included. Instead, this chapter gives a historical background of the research and events that led up to this thesis project.

2.2 Development of Platinum Silicide Focal Plane Arrays

Freeman Shepherd and Andrew Yang first proposed the use of internal photoemission from metal-silicide Schottky diode arrays for infrared imaging in a paper they coauthored in 1973 [27:310–313]. Since that time, significant advances in Platinum Silicide (PtSi) focal-plane arrays (FPAs) have resulted in the development of high resolution imaging devices for use in the 3 to 5 μm medium wavelength infrared (MWIR) band. Much of the work on PtSi FPAs has been accomplished under the direction of Dr. Shepherd (who holds the patent for the Schottky barrier focal plane array) at the Rome Laboratory (RL) [14, 24, 25, 26]. Early developments in PtSi FPAs are summarized in Table 1.

The 160 x 244 element FPA (last entry in Table 1) was first developed in 1983, and with improvements resulting in fill factors of better than 60% by 1987, it has been the most widely used PtSi device [13, 15, 16]. Since 1987, FPA resolutions of 320 x 244, 256 x 256, and 512 x 512 have been reported [12:11-25]. The most recent research has focused on 640 x 480 element FPAs.

2.3 Phillips Laboratory Involvement

The Airborne Measurements Branch at the Geophysics Direcorate of the Phillips Laboratory (PL/GD) is chartered to perform airborne measurements of the infrared properties of backgrounds and targets. These backgrounds and targets include both natural and man-made phenomena, such as natural earth backgrounds, natural sky backgrounds, aircraft emissions, and rocket plumes. To accomplish these measurements, PL/GD maintains the Flying Infrared Signatures Technology Aircraft (FISTA). The FISTA is a specially modified NKC-135 aircraft (serial number

Table 1. Reported Schottky-Barrier IR Focal Plane Arrays [13:1565]

TYPE OF FPA	*PIXEL SIZE* $(\mu m)^2$	*% FILL FACTOR*	*TYPE OF SBD*	*YEAR*	*COMPANY*
256 x 1 LINE SENSOR	40(H) x 320(V)	50	THICK-PtSi ψ_{ms} = [illegible] eV THIN-PtSi	1978 1980	RCA/RL RCA/RL
25 x 50 INTERLINE TRANSFER (IT)	160(H) x 80(V)	17	THICK-PtSi [illegible] THIN-PtSi	1978 1980	RCA/RL RCA/RL
32 x 63 SPS IT	160(H) x 80(V)	25	THIN-PtSi ψ_{ms} = .208 to 0.22eV THIN-Pd_2Si ψ_{MS} = 0.337eV	1981 1982	RCA RCA
64 x 128 IT	120(H) x 60(V)	22	THIN-PtSi ψ_{ms} = [illegible] to 0.22eV	1981	RCA
32 x 64 IT	133(H) x 80(V)	19	THIN-PtSi ψ_{ms} = 0.277eV	1981	Mitsubishi
256 x 1 LINE SENSOR	40(H) x 320(V)	50	THICK-PtSi ψ_{ms} = 0.27eV THIN-PtSi	1978 1980	RCA/RL RCA/RL
64 x 64 Meander-Channel IT	130(H) x 70(V)	23	THIN-PtSi ψ_{ms} = 0.23eV	1983	Fujitsu
256 x 256 IT	37(H) x 31(V)	25	THIN-PtSi ψ_{ms} = 0.26eV	1983	Mitsubishi
64 x 64 MOS	80(H) x 65(V)	58	THIN-PtSi ψ_{ms} = 0.23eV	1983	Mitsubishi
160 x 244 IT	80(H) x 40(V)	39	THIN-PtSi ψ_{ms} = 0.19 to 0.22eV	1983	RCA

55-3120) which carries a variety of spectral, radiometric, and spatial infrared instruments [20, 28].

In 1984, the Airborne Measurements Branch of PL/GD became interested in using a PtSi FPA IR camera as one of the instruments aboard the FISTA. In February of 1984, the initial airborne tests were conducted using a 64 x 128 pixel camera borrowed from RL. The 64 x 128 camera was flown again in the summer and fall of 1985 and proved to be a valuable instrument [32]. In 1986, a Memorandum of Agreement (MOA) was drawn up between RL and PL/GD for joint development of a 160 x 244 pixel PtSi camera for permanent use aboard the FISTA. The new camera first flew in 1987 and soon became one of FISTA's primary instruments [19].

The original 160 x 244 pixel PtSi camera used aboard FISTA consists of two main physical assemblies: the "camera head" and the "console." The camera head consists of a lens, the PtSi FPA device, a liquid nitrogen dewar, and control electronics. The camera head is supported by a moveable mount attached to the aircraft window. The outputs from the camera head include an analog signal containing all of the pixel information (carried on a 50 ohm coaxial cable), along with separate digital timing signals (carried on twisted pair cables). These signals are routed through the aircraft to the rack mounted console. In the console, the analog signal is sampled and converted to a 12-bit digital signal, level and gain are adjusted, image corrections are made, and the signal is formatted for display and recording.

Many modifications have been made to the original PL/GD 160 x 244 pixel PtSi camera in an effort to make the instrument more useful. These modifications include a remotely controlled filter wheel, addition of calibration data recording circuitry, replacement of analog gain and offset circuits with drift free digital circuits, and an improved analog-to-digital converter. One of the most recent modifications has been the 64 Mbit/Second Fiber Optic Image Transmission Link.

2.4 The 64 Mbit/Second Fiber Optic Image Transmission Link

Electromagnetic Interference (EMI) in the aircraft induces electrical noise into the analog signal along the cable path between the camera head and the console. The signal also suffers from attenuation over the length of the cable. The resulting corruption of the raw data signal is a significant problem. This problem, as well as new developments in small, low power analog–to–digital (A/D) converter technology, caused Mr. John Rex of PL/GD to propose moving the A/D converter from the console to the camera head [19]. The benefit of this arrangement is derived from the fact that once digitized, the signal is less susceptible to electrical noise corruption

during transmission to the console. Because of historical problems with long parallel digital data lines on aircraft [19], Rex also proposed converting the parallel data to a serial format at the camera head and transmitting the data to the console using optical fiber as the transmission medium. An additional benefit of using optical fiber is that it is insensitive to electromagnetic interference. Rex's ideas provided the basis for the fiber optic IR image transmission link.

The first IR image transmission link was designed and tested in 1989 using an optical fiber for the transmission medium at a link bit rate of 64 Mbits/second [18]. This link was demonstrated by using the output of the 160 x 244 pixel PtSi camera as input to the image transmission link, transmitting over a 50 foot optical fiber, and displaying the received data on a MaxScan (built by DataCube, Inc.) image processing system. A modified version of the original design has since been successfully incorporated by RL into a prototype PtSi IR camera system that is currently being flight tested for use aboard B-52 aircraft.

The initial success of the 64 Mbit/second IR Image Transmission Link, along with advances in the development of latest generation 640 x 480 PtSi IR cameras, prompted the proposal for a new-generation fiber optic IR image transmission link that would be compatible with higher resolution cameras. In 1990, PL/GD proposed that an Air Force Institute of Technology (AFIT) thesis project be devoted to investigation of the design of such an image transmission link. That proposal provided the basis for this thesis project.

III. Hardware Design

The fiber optic Image Transmission Link (ITL) consists of two separate printed circuit (PC) boards (a transmitter board and a receiver board) and a fiber optic cable. Each PC board is double sided. The transmitter board measures 7.5 inches by 6.0 inches, and the receiver board measures 9.0 inches by 5.5 inches. The two boards are connected by a single fiber optic cable. The input to the transmitter board is supplied by a Platinum Silicide (PtSi) Focal Plane Array (FPA) infrared imaging camera. The transmitter output is an optical signal which is transmitted over the fiber optic cable to the receiver board. The receiver board decodes the received optical signal and formats the image data for output to a digital image processor.

This chapter provides block diagram level details of the hardware design. Full schematic circuit diagrams, PC board layouts, etc. are provided in the appendix. The transmitter board, fiber optic cable, and receiver board are each treated separately.

3.1 The Transmitter Board

The input to the transmitter board comes from a PtSi FPA infrared imaging camera and is composed of five signals: 1) an analog image signal, 2) a digital pixel sample signal (which signifies valid pixel data on the analog image signal), 3) a digital horizontal synchronization signal, 4) a digital vertical synchronization signal, and 5) a digital even field signal (used to differentiate between even and odd fields when using interlaced video). The first two signals listed (the analog image signal and the digital pixel sample signal) are used by the transmitter to generate and transmit digital image information over the fiber optic cable. The last three signals listed (horizontal sync, vertical sync, and even field) are applied directly to the parallel-to-serial converter portion of the transmitter (see Section 3.1.3) for transmission to the receiver and are otherwise unused by the transmitter.

The transmitter board can be broken down into four parts (see Figure 1): 1) the Analog-to-digital (A/D) converter, 2) the transmitter pixel buffer, 3) the parallel-to-serial converter, and 4) the fiber-optic transmitter.

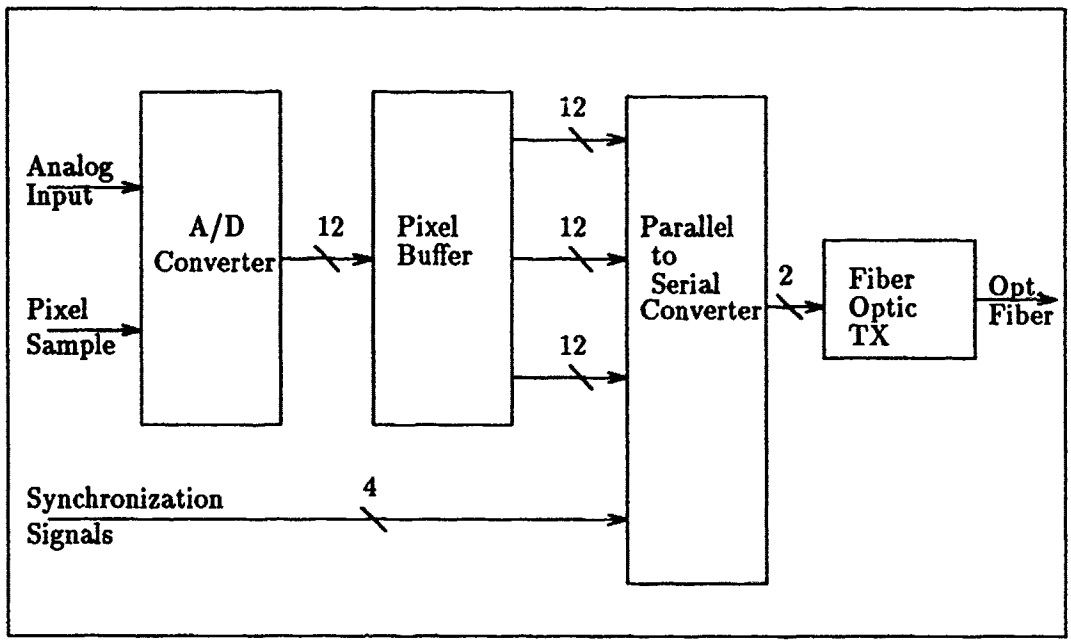


Figure 1. ITL Transmitter Board

3.1.1 The Analog-to-digital Converter The A/D converter is designed using the THC1202 12-bit A/D converter chip built by TRW [31]. The analog input to the THC1202 is supplied by the analog image signal from the infrared camera. On the rising edge of each pixel sample signal, the THC1202 samples the analog image signal and converts the samples to 12-bit digital numbers. Each 12-bit digital output from the THC1202 represents the intensity level of one pixel. The maximum sample rate of the THC1202 is 10^6 samples per second, which limits the maximum speed of the ITL to 10^6 pixels/second.

3.1.2 The Transmitter Pixel Buffer The transmitter pixel buffer takes the 12-bit pixels from the A/D converter and formats them for input to the parallel-to-serial converter. The parallel-to-serial converter requires a 40-bit parallel input (see next section). The pixel buffer creates a 36-bit parallel output by combining three 12-bit pixels. Four synchronization bits (horizontal sync, vertical sync, even field, and a spare) are then added to the output of the pixel buffer to create the required 40-bit parallel input to the parallel-to-serial converter.

Digital 12-bit pixel data from the A/D converter is latched into the transmitter pixel buffer 80 ns after each pixel sample signal. This pixel data is then simultane-

ously provided to the inputs of three separate 12-bit data latches called LATCH1, LATCH2, and LATCH3 (see Figure 2). The three data latches are clocked one at a time, with one data latch being clocked for each pixel sample signal. The outputs of the three 12-bit data latches are applied in parallel to the input of the parallel-to-serial converter. After all three data latches have latched in their separate pixels, a strobe signal is sent to the parallel-to-serial converter to signify that the data is ready.

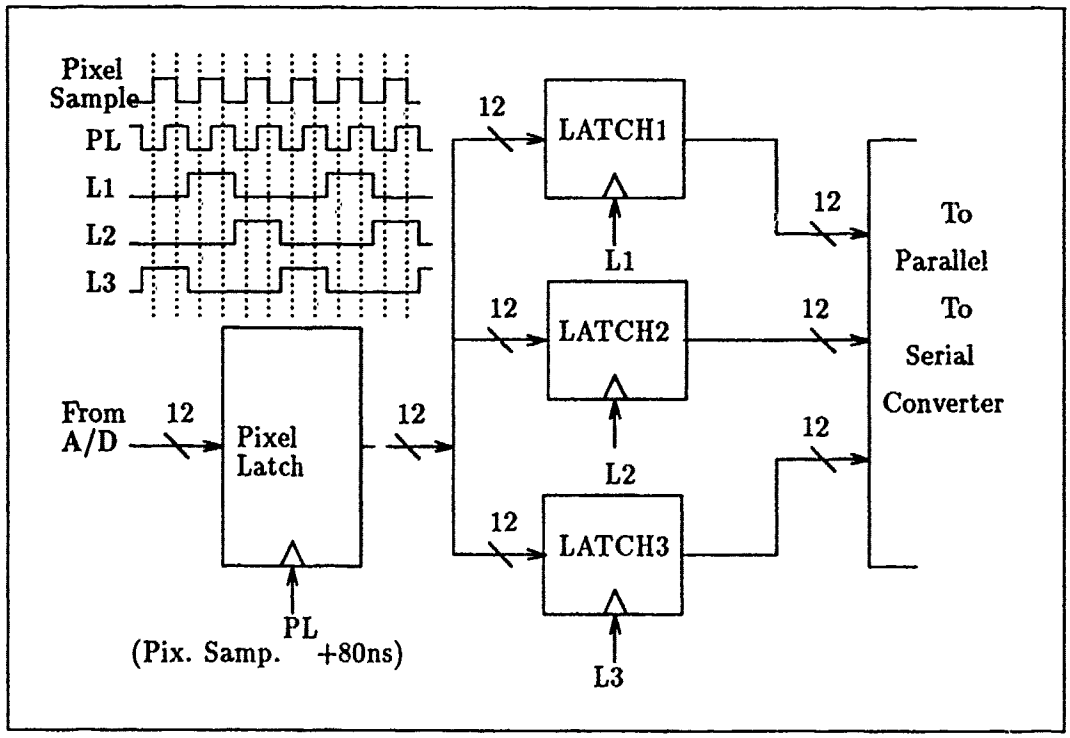


Figure 2. Transmitter Pixel Buffer

Timing for the transmitter pixel buffer is generated using a tapped digital delay circuit along with a two flip-flop (4 state) state machine. The tapped digital delay circuit is implemented using a DDU-224F-200 digital delay unit manufactured by Data Delay Devices, Incorporated [6] which is driven by the pixel sample signal. The tapped digital delay circuit produces delayed copies of the pixel sample signal at delays of up to 200 nanoseconds (ns) in increments of 20 ns. The 80 ns tap is used to latch data from the A/D converter. The 120 ns tap drives the two flip-flop state machine which sequentially generates clock signals for LATCH1, LATCH2, and

LATCH3 (the transmitter state machine uses only three of the four possible states). The parallel-to-serial converter strobe is derived from the LATCH3 clock and the 200 ns tap.

3.1.3 The Parallel-to-serial Converter Design of the parallel-to-serial converter centers around the GA9011 HOT ROD^{TM} gallium arsenide transmitter built by Gazelle Microcircuits [9]. The GA9011 is designed to accept 40-bit parallel data words as input at rates of up to 25×10^6 40-bit words per second. For purposes of the ITL, the 40-bit words are made up of three 12-bit pixels in parallel, with the extra four bits connected directly to the horizontal sync, vertical sync, even field, and spare inputs from the infrared camera. Within the parallel-to-serial converter, the 40-bit words are each split up into ten 4-bit nibbles and each nibble is encoded into a 5-bit code symbol for serial transmission. The conversion from 4-bit nibbles to 5-bit code symbols results in 50 bits of serial data for each 40-bit input data word (To avoid confusion with the input data bits, the encoded serial data bits are referred to as 'bauds' by the GA9011 manufacturer. In this thesis, however, the encoded serial data bits will be referred to as 'code bits'). The encoded data bits are transmitted serially over a differential pair of 50-ohm output lines in a Non-Return-to-Zero, Invert-on-ones (NRZI) format. The serial data rate is thus:

$$\text{(pixel rate)} \times \text{(40 data bits/3 pixels)} \times \text{(50 code bits/40 data bits)} \qquad (1)$$

Using this equation, the serial bit rate at the maximum input pixel rate of 10^6 pixels/second is calculated to be 166.7×10^6 bits per second. The GA9011 is designed to run at a minimum serial bit rate of 250×10^6 bits per second. In the ITL system, extra synchronization bits are inserted in order to increase the apparent serial bit rate of 166.7×10^6 bits per second up to the minimum required by the GA9011.

3.1.4 The Fiber Optic Transmitter The fiber optic transmitter is implemented using the AT&T 1252N light emitting diode (LED) fiber optic transmitter circuit [3]. The 1252N is physically located as close as possible to the output of the parallel to serial converter (and the inputs are terminated at 50-ohms) in order to minimize the effect of reflections in the 250 Mbit/sec serial waveform. The output of the 1252N is a pulsed optical waveform at a wavelength of 1.3 μm which interfaces directly to a fiber optic cable through an AT&T ST^{TM} connector. The 1252N is rated for a

maximum bit rate of 220 Mbit/sec, but it is driven at 250 Mbit/sec (the minimum recommended serial bit rate for the parallel to serial converter). AT&T tests have shown that the 1252N is capable of operation at 250 Mbit/sec with a power margin penalty of approximately 1.5 dB [5].

3.2 The Fiber Optic Cable

The fiber optic cable used for ITL testing is built by AT&T. It contains a single multi-mode optical fiber with core/cladding diameters of 62.5/125 μm and a numerical aperture of 0.29. A 50 foot length of cable was used for testing the ITL. The attenuation rating of the cable is 1.0 dB/km (max) and the bandwidth–distance product is 500 MHz–km (max). Each end of the cable is fitted with an AT&T ST^{TM} connector with a rated loss of 0.5 dB per connector.

3.3 The Receiver Board

The only input to the ITL receiver board is the optical output of the fiber optic cable. The outputs from the receiver board are intended to interface directly with a MaxVideo^{TM} image processor built by DataCube, Inc. and include four separate output signals: 1) 12-bit parallel pixel data, 2) a pixel output clock (which signifies valid pixel data), 3) a horizontal synchronization signal, and 4) an interlaced vertical synchronization signal (synthesized from the even field and vertical sync signals transmitted from the infrared camera).

The receiver board can be broken down into five parts (see Figure 3): 1) the fiber optic receiver, 2) the serial-to-parallel converter, 3) the receiver pixel buffer, 4) the vertical sync delay circuit, and 5) the vertical sync interlace circuit. Each part of the receiver board will be described separately.

3.3.1 The Fiber Optic Receiver The fiber optic receiver was implemented using the AT&T 1352N fiber optic receiver circuit [3]. The input to the 1352N is a pulsed optical signal coupled into the circuit through an AT&T ST^{TM} fiber optic connector. The output of the 1352N is transmitted serially over a differential pair of 50-ohm output lines to the serial-to-parallel converter. Due to the high data rates (250 Mbit/sec) the 1352N is physically located as close as possible to the input of the serial-to-parallel converter (and the output lines are terminated at 50-ohms) in order to minimize the effect of reflections in the serial waveform.

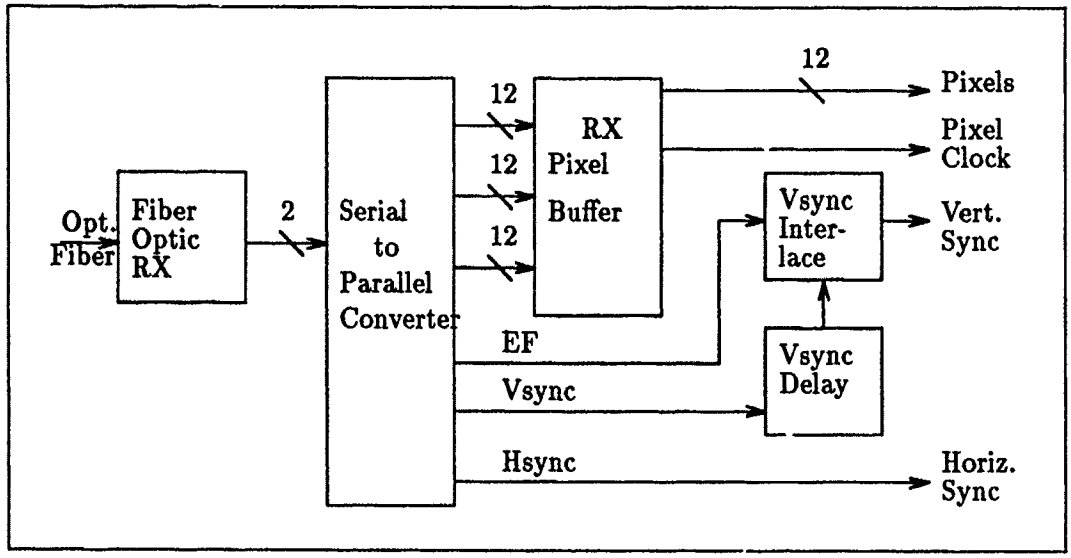


Figure 3. ITL Receiver Board

3.3.2 The Serial-to-parallel Converter Design of the serial-to-parallel converter centers around the GA9012 HOT ROD^{TM} gallium arsenide receiver built by Gazelle Microcircuits [9]. The GA9012 is designed to accept serial data over a differential pair of 50-ohm lines in a Non-Return-to-Zero, Invert-on-ones (NRZI) format. The serial data is received in blocks of 50 code bits, the NRZI format is decoded, and then the 50-bit blocks are broken up into ten 5-bit code words. Each 5-bit code word is decoded into a 4-bit data nibble and then the ten 4-bit nibbles are output as a 40-bit parallel data word. For purposes of the ITL, the 40-bit words are made up of three 12-bit pixels with the extra four bits carrying horizontal sync, vertical sync, even field, and a spare signal from the infrared camera. A 'data strobe' output from the GA9012 is asserted whenever a new 40-bit output is valid.

The GA9012 is capable of limited error detection. The mapping of the 4-bit data nibbles into 5-bit code words leaves 16 of the 32 possible 5-bit code words unused (they may be used for other purposes, such as synchronization, but they do not represent valid data). If an invalid 5-bit code word (one that does not represent valid data) is detected during decoding from code words to 4-bit data nibbles, then an 'error' line on the GA9012 is asserted and the offending code word is decoded as a 1111 data nibble. In the ITL receiver, the GA9012 'error' line causes a red light emitting diode (LED) to light up for approximately one-fourth of a second,

indicating reception of an erroneous code word. It is possible that one or more bits in a 5-bit code word may be changed during transmission (due to noise). If bit errors cause a code word to change to another of the 16 possible valid code words, then the errors go undetected. The receiver board provides no means to output error indications, however, and erroneous data nibbles are output in the same manner as valid data nibbles.

3.3.3 The Receiver Pixel Buffer The receiver pixel buffer acts as the interface between the 40-bit parallel output of the serial-to-parallel converter and the output of the receiver board (see Figure 4). The output of the receiver board is intended to interface directly to a MaxVideo^{TM} image processor system built by DataCube, Inc. (hereafter referred to as the 'DataCube System') which requires the 12-bit pixels to be presented one at a time at a maximum rate of 10^6 pixels per second [7].

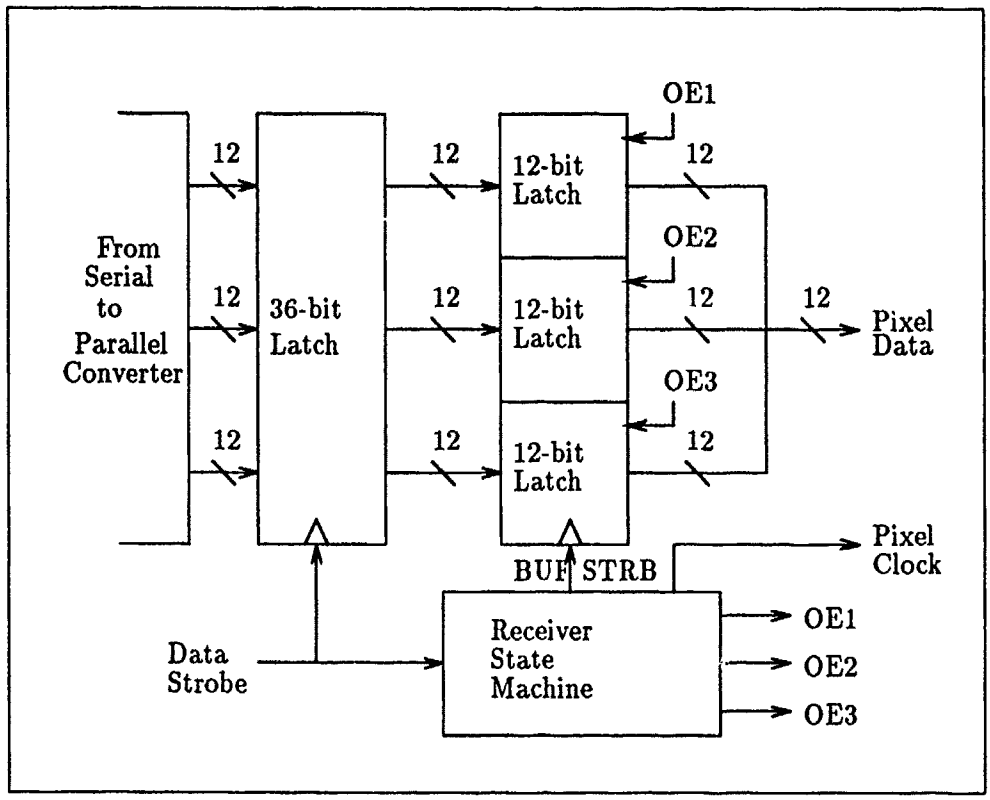


Figure 4. Receiver Pixel Buffer

The maximum rate at which the transmitter board is designed to send pixels is 10^6 pixels per second (limited by the A/D converter). At this rate, 40-bit parallel

data words will arrive at the output of the serial-to-parallel converter unevenly in time. The uneven arrival times are due to the mismatch between the minimum 40-bit word rate of the GA9011/GA9012 (5×10^6 40-bit words per second) and the rate at which the 40-bit words are generated by the transmitter pixel buffer (10^6 pixels/sec $\times 3$ pixels per 40-bit word $= 3 \times 10^6$ 40-bit words per second). When pixels are being sent at 10^6 pixels per second, two 40-bit parallel data words will arrive at the output of the serial-to-parallel converter 200 ns apart, followed by an interval of 400 ns before the arrival of the third. Since the maximum rate at which the image processor can accept pixels is 10^6 pixels per second (100 ns between pixels), and each 40-bit parallel data word contains three pixels, 300 ns are required in order to output the pixel data in one 40-bit parallel data word. While 300 ns is the average time between arrival of 40-bit data words, the instantaneous timing may be as short as 200 ns. The receiver pixel buffer solves this problem by providing an extra latch where parallel data from the serial-to-parallel converter may be stored until the image processor is ready.

Thirty-six bits of the parallel 40-bit data from the serial-to-parallel converter are latched into the first of two 36-bit latches on the rising edge of the data strobe signal (the other 4 bits are latched into a separate 4 bit latch for use as synchronization signals). The data strobe signal is generated by the serial-to-parallel converter and signifies that valid data is ready. The outputs from the first 36-bit latch are connected directly to the inputs of the second 36-bit latch. The second 36-bit latch is arranged into three separate sub-units of 12-bits each. The 12-bit outputs of each sub-unit are hard wired together in bus fashion to form a single 12-bit output bus. The outputs on each of the three 12-bit sub-units can be placed in a high impedance 'tri-state' mode so that only one of the sub-units is driving the bus at a time. The timing of the data transfers from the first 36-bit latch to the second 36-bit latch and from the second 36-bit latch to the 12-bit output bus is controlled by the receiver state machine.

The receiver state machine is implemented using two flip-flops for a total of four possible states. Timing signals generated by the receiver state machine include BUFSTRB (which controls the latching of data into the second 36-bit latch) and PIXELCLK (which is an output from the receiver board indicating that valid pixel data is ready). Also generated by the receiver state machine are OE1, OE2, and OE3, which are the output enable signals that control which of the three 12-bit pixels is placed on the output bus.

The idle state for the receiver state machine is state 00. In this state, all three 12-bit sub-units of the second 36-bit latch are placed in the high impedance state (OE1, OE2, and OE3 are all high), so that the output bus is left floating. BUFSTRB and PIXELCLK stay low. The state machine remains in this state until a data strobe signal is detected from the serial-to-parallel converter. The data strobe signal causes the first 36-bit latch to latch the output data from the serial-to-parallel converter and causes the state machine change to state 01 on the next clock cycle.

In state 01, the state machine generates a BUFSTRB signal which latches data from the outputs of the first 36-bit latch into the second 36-bit latch. State 01 drives OE1 low (while holding OE2 and OE3 high), which puts data from the first 12-bit pixel onto the output bus. PIXELCLK is enabled. After state 01, the state machine will change to state 10 on the next clock cycle.

In state 10, BUFSTRB is held low and PIXELCLK is enabled. OE2 is driven low (while OE1 and OE3 are held high), which puts data from the second 12-bit pixel onto the output bus. After state 10, the state machine will change to state 11 on the next clock cycle.

In state 11, BUFSTRB is held low and PIXELCLK is enabled. OE3 is driven low (while OE1 and OE3 are held high), which puts data from the third 12-bit pixel onto the output bus. After state 11, the state machine will change to state 01 if a new data strobe has been detected (indicating that another 40-bit data word is waiting) or to state 00 otherwise.

By using two 36-bit data latches along with the timing generated by the receiver state machine as described above, the receiver pixel buffer is able to separate the output of the serial-to-parallel converter into separate pixels. The pixel buffer then delivers the pixel data to the output of the receiver board at the rates required by the image processor.

3.3.4 The Vertical Sync Delay Circuit The vertical synchronization timing requirements for the DataCube image processor system are incompatible with the vertical synchronization signal transmitted by the infrared camera. The purpose of the vertical sync delay circuit is to rectify the timing problem.

In order for the DataCube system to catch the first line of pixels in a frame, the vertical sync signal must occur 4 lines before the beginning (line 1) of the frame

[18]. The vertical sync signal from the infrared camera occurs just prior to the start of a new frame, with no horizontal lines between the vertical sync and line 1 of the new frame [18]. If the vertical sync timing is left unchanged, then the first four lines of the even and odd fields will be lost (eight lines total). This problem is solved by the vertical sync delay circuit.

The vertical sync delay circuit consists of a 12-bit, presetable, binary counter. The vertical sync signal from the serial link receiver presets the counters to a binary number which is set using a series of DIP switches. The number set on the switches should be 4 less than the number of lines per field. The counters then count down on horizontal sync signals. When the counter counts down past 0000 0000 0000 to 1111 1111 1111, the circuit generates the delayed vertical sync pulse. Assuming proper DIP switch settings, the delayed pulse actually becomes an advanced pulse for the following field.

On the ITL receiver board, the three most significant bits of the 12-bit vertical sync delay counter are hard-wired low, and the other nine bits are controlled by DIP switches (see Figure 5). This allows delays of up to $2^9 = 512$ lines which is sufficient for focal plane arrays with 516 lines or less (including the 640 x 480 array).

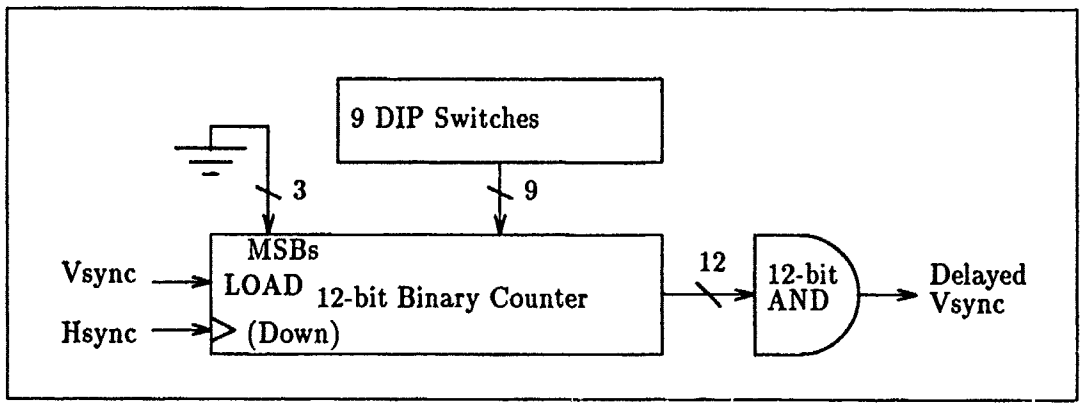


Figure 5. The Vertical Sync Delay Circuit

3.3.5 The Vertical Sync Interlace Circuit In interlaced video each frame of data is made up of an even and an odd field. The odd field consists of all of the odd lines in the frame (1,3,5, etc.) and the even field consists of all the even lines in the frame (2,4,6, etc.). To make up a complete frame, one of the fields is displayed

entirely and then lines from the second field are displayed between the lines of the first. The key point is that the system used to display the data must be told: 1) whether the data to be displayed is interlaced or not, and 2) if the data is interlaced, which is the odd field and which is the even field. This information is conveyed to the DataCube image processor system through the timing relationship between the vertical sync signal and the horizontal sync signal (details of DataCube vertical sync timing are given in [18]).

The vertical sync interlace circuit on the ITL receiver board uses the output of the vertical sync delay circuit (section 3.3.4) and the even field signal (received from the infrared camera) to synthesize an interlaced vertical sync signal. A DIP switch is provided on the ITL receiver board to select either the non-interlaced vertical sync (the output of the vertical sync delay circuit) or the interlaced vertical sync for use as the vertical sync output to the DataCube system. The vertical sync interlace circuit used by the ITL receiver is a duplicate of the circuit used in [18], which contains a detailed discussion of circuit operation.

3.4 Summary

Hardware design for the image transmission link is tied directly to the GA9011 and GA9012 HOT ROD^{TM} chip set and the AT&T 1252N and 1352N fiber optic components. This chapter has shown that by using these components it is possible to design an image transmission link that meets the size and speed requirements of the infrared camera system. In the next two chapters (Determination of Success Criteria and Theoretical Performance Predictions) it will be determined whether this design can meet the noise and bit error rate requirements of the infrared camera system.

IV. Determination of Success Criteria

4.1 Introduction

Success, for the Image Transmission Link (ITL), is based on the ability to transmit image data without adding significant quantities of noise relative to noise levels already present prior to transmission. The concept of significant versus insignificant noise and how the noise effects the classification of an ITL system as successful or unsuccessful is the subject of this chapter.

Ideally, the ITL would be completely "invisible", meaning that a close examination of a set of image data would not reveal whether the data was recorded before or after transmission by the ITL (in such a situation the ITL noise would be insignificant). This level of performance will be classified as "absolute success". The criteria for achievement of absolute success is defined in detail later in this chapter. The concept of absolute success is interesting and provides insight into the relationship between the noise inherent in the image prior to transmission and the noise introduced by the ITL. It will be shown, however, that the criteria for absolute success are overly restrictive and consequently impractical. A less restrictive definition of success, classified as "practical success", will be defined and used as the basis for determining the success or failure of the ITL.

4.2 Focal Plane Array Operation

The platinum silicide (PtSi) focal plane arrays (FPAs) for which the ITL is designed are each constructed from a single silicon wafer and operate as a charge coupled device (CCD) [13]. The 307,200 individual detectors in a 640 x 480 element FPA are arranged rectangularly with 480 horizontal rows of 640 detectors. Each detector consists of a PtSi Schottky photodiode which is sensitive to infrared radiation in the 1 to 5 μm wavelength range [25]. A lens is used to focus an image onto the detector array and each detector emits photoelectrons at a rate proportional to the intensity of the radiation incident upon it. Photon arrival and photoelectron emission/detection can be modeled as a random event described by Poisson statistics [15]. The photoelectrons from each detector are collected in areas of the silicon called "potential wells" adjacent to the photodiodes. Collection time (also called integration time) is 1/30 of a second (one standard video frame time) after which

the charge from each detector is transferred through standard CCD techniques [13] to the output node of the detector array. At the output node, the charge collected by each detector is read out sequentially and converted to a proportional analog voltage waveform. Separate digital data lines carry vertical, horizontal, and pixel synchronization pulses that signal the beginning of each frame, horizontal line, and pixel.

In a typical CCD device the output node is located at the upper left corner of the rectangular array [8]. Charge is moved to the output node through a cyclic pattern of transfers controlled by voltage changes on strategically placed electrodes. First the charge corresponding to the topmost row of detector elements is read out, starting with the leftmost detector, by repeatedly transferring charge one position to the left. Then charge is transferred from each horizontal row to the row above and the topmost row is again read out. The process continues until charge corresponding to all pixel elements has been read out, and then the next frame begins. As a result of the charge transfer process, the charge at each detector position of the array experiences a different number of transfers before reaching the output node.

It is convenient to refer to detector locations by their row and column numbers. Each location is uniquely identified by a pair of numbers, with the first representing the row number (starting at the top) and the second representing the column number (starting at the left). (1,1) corresponds to the upper left position, (480,1) to the lower left, (480,640) to the lower right, and so on. Using this notation it can be seen that the charge at location (1,1) is transferred only once before it reaches the output node, while the charge at location (480,640) experiences the maximum number of 1,119 transfers (479 vertical transfers plus 640 horizontal transfers).

The analog voltage at the output node of the focal plane array is amplified, sampled at each detector output time, and then converted to a sequential series of 12–bit binary numbers, one for each detector in the array. In many cases it is useful to consider output level of the individual detectors in terms of analog–to–digital converter units (ADUs). For the 12–bit system, each detector output can be quantized to $2^{12} = 4096$ levels, or equivalently, each detector element takes on a value from 0 to 4095 ADUs. For a given amount of charge at the output node, the corresponding digital signal output of the analog–to–digital (A/D) converter is given by [15]

$$S = GN \tag{2}$$

where S is the digital output signal level in ADUs, G is the gain associated with the amplifier and A/D converter in ADUs/electron, and N is the charge at the output node in electrons (each electron carries 1.602×10^{-19} Coulombs of charge). Murguia[15] measured the value of G^{-1} on a 160 x 244 element PtSi focal plane array camera as 218 electrons/ADU. Data is not yet available on the 640 x 480 element camera, but output and A/D circuitry are sufficiently similar that this value can be treated as a good approximation for the 640 x 480 system.

The sources of noise in the focal plane array can be represented by three significant quantities: shot noise, electronics noise, and spatial noise. Shot noise and electronics noise are temporal in nature (random in time). Shot noise is produced by random variations in photon arrival/detection and can be described by Poisson statistics. Electronics noise is associated with charge transfer, clock pickup, amplifiers, and drive electronics. Spatial noise is produced by random non-uniformities in individual detector elements over the spatial extent of the array.

4.3 Shot Noise Characteristics

The relationship between photons arriving at a detector and the photoelectrons emitted can be modeled as a Poisson random process. The probability that N photoelectrons will be emitted in a time interval τ is given by [23:132]

$$P(N) = \frac{(\lambda\tau)^N}{N!} e^{-\lambda\tau} \tag{3}$$

where λ is the rate function and is determined by the rate of photon arrival as well as the gain characteristics of the detector. In a Poisson process

$$\overline{N} = \sigma_N^2 = \lambda\tau \tag{4}$$

where $\overline{N}$ is the mean value of emitted photoelectrons and σ_N^2 is the variance [23:131-132]. Equation (4) shows that as the incident radiation intensity increases, λ increases, causing an increase in signal level (proportional to $\overline{N}$) and a corresponding increase in noise (represented by σ_N^2).

Once the Poisson-distributed quantity of charge has been collected, it must be transferred to the output node of the detector array. The charge transfer is not 100% efficient. Each transfer leaves a finite amount of charge behind which is

picked up by the following group of charge. Also, some of the charge is lost to bulk recombination in the process of each transfer. The average fractional amount of charge that is transferred during each charge transfer operation is referred to as the charge transfer efficiency (CTE).

The Poisson distribution of the charge quantities is distorted in a non-linear fashion for charge quantities that experience a large number of transfers. The distribution remains intact for detectors located close to the output node, however, and the total shot noise at the output of the A/D converter can be approximated by [15]

$$\sigma_{shot(out)} = G^2 \sigma_{N'}^2 \tag{5}$$

where $\sigma_{shot(out)}$ is the total shot noise at the output of the A/D converter, G is the gain as defined in Equation (2), and $\sigma_{N'}^2$ is the variance of N' (the number of collected photoelectrons, N, that reach the output node. For pixels located close to the output node, $\sigma_{N'}^2 \approx \sigma_N^2$).

4.4 Electronics Noise Characteristics

Electronics noise is the term used to describe the sum of the noises produced by the electronic devices and circuits used to operate the detector array. This noise is associated with a large number of random thermal and other effects occurring in the processes of charge transfer, clock pickup, amplification, and so forth. According to the central limit theorem [17:194-200] the probability density function of the sum of a large number of independent random variables approaches the Gaussian density function. The electronics noise can be modeled as a zero mean additive white Gaussian noise process with probability density function

$$P(n) = \frac{1}{\sqrt{2\pi\sigma_f^2}} \exp\left(-\frac{1}{2}\frac{n^2}{\sigma_f^2}\right) \tag{6}$$

where n is the amplitude of the noise, σ_f^2 is the variance of the electronics noise, and $P(n)$ is the probability that the noise is of amplitude n [29:28].

The variance of the electronics noise at the output of the A/D converter on a

160 x 244 element PtSi focal plane array camera has been measured as [15]

$$G^2\sigma_f^2 = 4 \text{ ADUs} \tag{7}$$

which is a reasonable approximation for the 640 x 480 element camera.

4.5 Spatial Noise Characteristics

Ideally every detector element in the focal plane array would be identical. In practical arrays, however, individual detector characteristics vary randomly with spatial position in the array. The most fundamental variations occur in the gain (responsivity) and offset (dark current) characteristics of the detector elements [15]. Detector gain is the ratio of average radiation intensity incident at the detector to the rate of photoelectron emission by the detector. Detector offset can be defined as the expected number of electrons which accumulate due to dark current (current which flows in the absence of incident radiation) during the frame time. Detector gain and offset are two of the fundamental quantities effecting the value of the rate factor (λ) described in equation (3). Spatial noise varies linearly with the intensity of incident radiation and becomes the dominant noise form for high intensity levels [14]. Spatial noise can be reduced through gain and offset correction techniques [15, 14].

4.6 Noise Limited Operation of the Focal Plane Array

A simplified expression for the total system noise at the output of the A/D converter can be written

$$\sigma_{tot}^2 = G^2\sigma_{N'}^2 + G^2\sigma_f^2 + G^2\sigma_s^2 \tag{8}$$

where σ_{tot}^2 is the variance of the total system noise at the output of the A/D converter in ADUs, σ_f^2 is the variance of the electronics noise at the output node, $\sigma_{N'}^2$ is the variance in the number of electrons reaching the output node (shot noise), σ_s^2 is the variance of the spatial noise at the output node, and G is the gain as defined in Equation (2).

Shot noise and spatial noise increase with increasing incident radiation intensity, while electronics noise is independent of incident radiation. Also, the distribution of the shot noise is effected by the number of charge transfers and is unique for

each detector. At low radiation intensity levels, electronics noise dominates. Shot noise dominates at medium intensity levels and spatial noise dominates at higher radiation levels [14]. The exact values of shot noise, spatial noise, and electronics noise vary from camera to camera, but the general relationship between these quantities is illustrated in Figure 6.

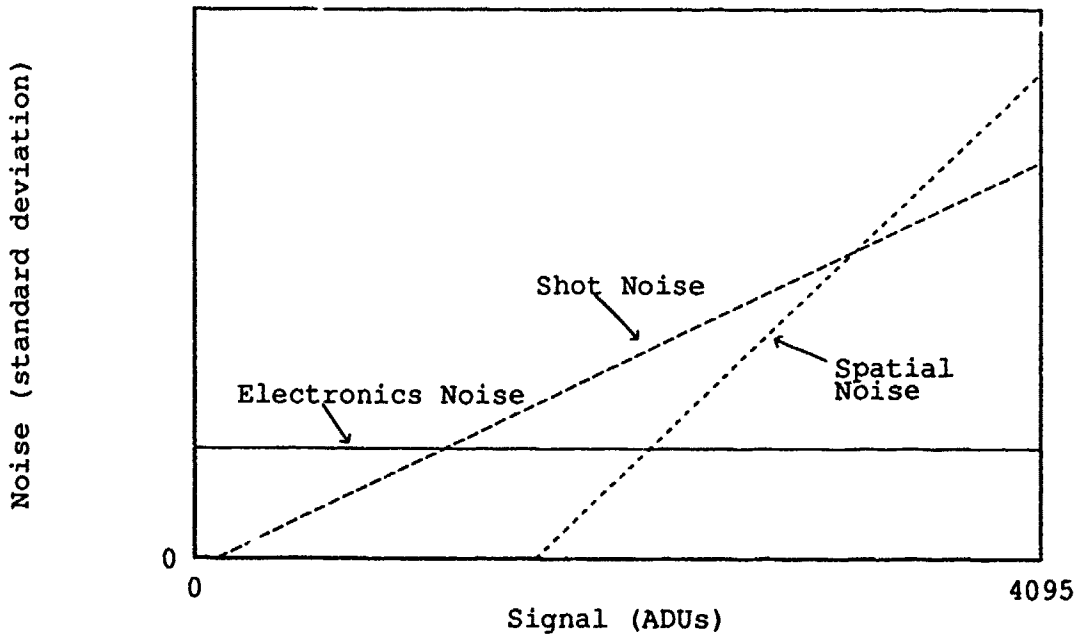


Figure 6. Electronics, shot, and spatial noises vs. signal intensity [14]

The distribution of the noise introduced by the ITL does not vary with variations in incident intensity. It is independent of the shot noise, spatial noise, and electronics noise (the distribution of the ITL noise is discussed in detail in Chapter V).

In practice, the ITL is required to transmit images which vary over the full range of incident radiation intensity. Ideally the distribution of the noise introduced by the ITL during transmission will be sufficiently less (within the full 0 to 4095 ADU range of possible transmitted values) than the distribution of the noise inherent in the image before transmission that the ITL noise will be virtually undetectable in the received image. If this is to be true for all images and all incident radiation intensities, then the distribution of the ITL noise must be arbitrarily lower in magnitude than the lowest possible level of noise inherent in any particular image prior to transmission.

From Figure 6, the low-noise limit in pre-transmission images occurs in low incident radiation images (where electronics noise dominates).

A model of the pre-transmission image noise in the low-noise limited region may be developed for comparison to noise introduced during image transmission. Since the low-noise limit is determined by the electronics noise, the shot noise and spatial noise will not affect the model, and the model can be based exclusively on the electronics noise.

In Section 4.4 it was shown that the electronics noise can be modeled as a zero mean, additive, Gaussian process with a variance of approximately 4 ADUs. The electronics noise has a continuous, Gaussian distribution at the input to the A/D converter. The A/D converter has the effect of quantizing the electronics noise into a discrete probability distribution. The equation for the continuous Gaussian probability distribution of the electronics noise (Equation 6) is integrated over the range of each quantization level to convert to a discrete probability distribution function. The probability that the magnitude of the error due to quantized electronics noise will be equal to a particular integer number of ADUs can thus be written

$$P(|\text{error}| = E_r) = 2\int_{E_r-0.5}^{E_r+0.5} \frac{1}{\sqrt{2\pi(4)}} \exp\left(-\frac{1}{2}\frac{n^2}{(4)}\right) dn \tag{9}$$

where E_r is the particular integer number of ADUs and the limits of integration are due to the quantization process (pre-quantization signal levels in the range from $E_r - 0.5$ to $E_r + 0.5$ are converted to the single post-quantization value E_r). In terms of the Complementary Error Function, $Q(x)$

$$P(|\text{error}| = E_r) = 2\left[Q\left(\frac{E_r - 0.5}{2}\right) - Q\left(\frac{E_r + 0.5}{2}\right)\right] \tag{10}$$

where $Q(x)$ is defined as

$$Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{n^2}{2}\right) dn \tag{11}$$

and tabulated values of $Q(x)$ can be found in Reference [29:742] and many other mathematics references.

The probabilities defined by Equations (9) and (10) are based on the distributions of the minimum noise limited performance of the detector array. Comparisons of these probabilities with noise induced by the ITL require calculations involving large values of E_r. Calculations involving values of E_r larger than 10 generally require approximations. $Q(x)$ can be approximated by [17:47–48]

$$Q(x) \approx \frac{1}{x\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) \quad \text{(For large x)} \tag{12}$$

An approximation for the logarithm of $P(|\text{error}| = E_r)$ can be derived from Equation (10) by approximating the value of $Q[(E_r - 0.5)/2] - Q[(E_r + 0.5)/2]$ as $1/\sqrt{8\pi} \times \exp(.99E_r)^2/8$ (derived empirically by the author) and taking the logarithm of both sides. The result is given by

$$\log P(|\text{error}| = E_r) = -(0.39909 + 0.05321E_r^2) \tag{13}$$

4.7 Absolute Success Criteria

Absolute success is achieved by the ITL when the distribution of the noise magnitude induced by the ITL is arbitrarily less than the distribution of the noise magnitude induced by the detector array for all possible values of noise magnitude (E_r). This definition of absolute success criteria can be stated mathematically as

$$\frac{P(|\text{error}_{ITL}| = E_r)}{P(|\text{error}_{Array}| = E_r)} \leq k \quad , \forall E_r \tag{14}$$

where k is an arbitrarily small number and $\forall E_r$ means 'for all values of E_r'. Choosing 1% as the value of k ($k = 0.01$) and taking the logarithm of both sides of equation (14) yields (using Equation (13) for the value of $P(|\text{error}_{Array}| = E_r)$)

$$\log P(|\text{error}_{ITL}| = E_r) \leq -(0.39909 + 0.05321E_r^2) - 2 \quad , \forall E_r \tag{15}$$

which can be applied directly to a given distribution of ITL noise in order to determine strict compliance with absolute success criteria.

While the conditions defined for absolute success are strictly correct, they impose impractical restrictions on ITL performance. This can be illustrated by

considering that, in a generalized 12-bit digital system, any bit is just as likely to be in error as any other (a uniform probability distribution). An error in the most significant bit (a 2,048 ADU error) is, therefore, just as likely as an error in the least significant bit (a 1 ADU error). Applying equation (15) with $E_r = 2,048$ ADUs requires the ITL to have a probability of bit error less than $10^{-223,181}$ if it is to be classified as successful. Such a bit error rate translates to one bit error every $10^{223,165}$ years, a level of performance that would be virtually impossible to verify.

As stated in the introduction to this chapter, the concept of absolute success is interesting and provides insight into the relationship between the noise inherent in the image prior to transmission and the noise introduced by the ITL. If the success of the actual ITL system is to be judged, however, a different set of success criteria must be developed.

4.8 Practical Success Criteria

A more practical approach to the problem of determining success criteria may be developed by considering the manner in which the image data is to be used. In actual operation of the PtSi camera, image frames are displayed in real time on an operator's monitor and recorded on analog tape for later analysis. Random pixel errors in the real time display are virtually undetectable by the human eye as long as the number of pixel errors per frame is relatively small. When the recorded data is carefully analyzed on a frame by frame basis, however, pixel errors of large magnitude can be detected. If the pixel error rate is low relative to the frame rate, then the few erroneous pixels which occur in each frame are seldom of any consequence. This is because the region of interest usually occupies only a fraction of the image frame, and consequently there is some reasonable probability that the erroneous pixel will occur outside the region of interest. If, for example, the region of interest occupies 50% of the pixels in a frame, then there is a 50% probability that it will interfere with the object of interest. Assuming an erroneous pixel does occur at a critical location, then the previous or following frame can generally be used with good results.

Equation (14), which was used to define absolute success, can be used to define two regions of error performance in the transmitted data. Using this equation with $k = 1$ establishes the point where the array noise level and the ITL noise level are equal. This point is defined as the noise division threshold γ_N. γ_N occurs at the value of error magnitude $E_r = \gamma_N$ where $P(|\text{error}_{ITL}| = \gamma_N) = P(|\text{error}_{Array}| = \gamma_N)$.

The region of error magnitudes greater than γ_N is dominated by ITL noise, while the region of error magnitudes less than γ_N is dominated by array noise as illustrated in Figure 7. Because of these regions of domination, pixel errors of magnitude less than γ_N are likely due to detector array noise, while pixel errors of magnitude greater than γ_N are more likely due to ITL noise.

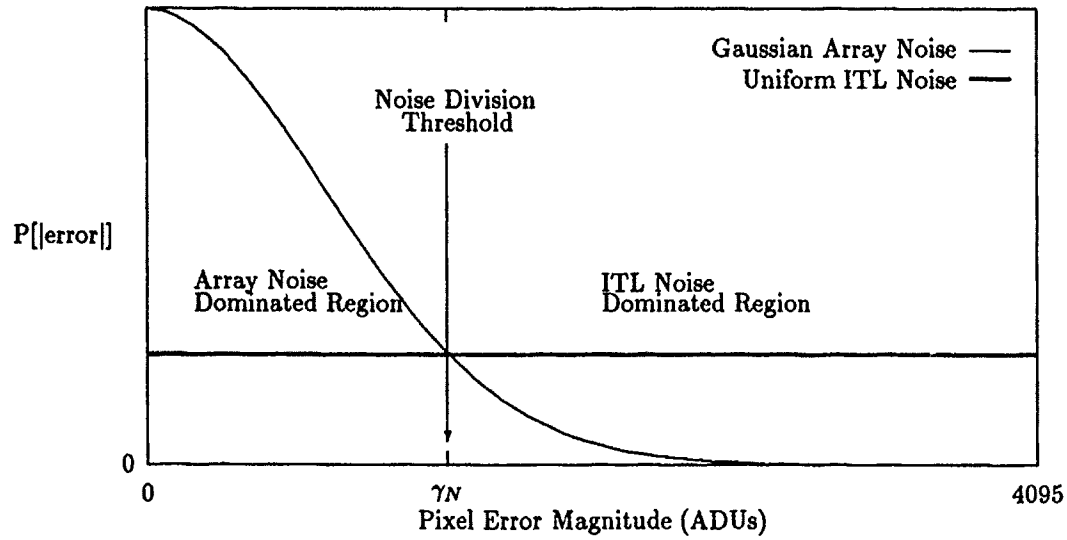


Figure 7. Gaussian Array Noise vs. Uniform ITL Noise

Achievement of practical success is based on the fact that errors in the ITL noise dominated region of error performance will tend to occur at a much slower rate than errors in the array noise dominated region. The distribution of the detector array noise is such that more than 75% of the pixels include additive noise errors of one to four ADUs in magnitude (more than 75% of the area under the Gaussian curve occurs between $-\sigma$ and $+\sigma$, with $\sigma = 4$ ADUs in this case). Array noise errors of four ADUs or less are small enough in magnitude that they are difficult to detect. Errors in the ITL noise dominated region occur much less frequently, but are of sufficient magnitude that they may be catastrophic to the affected pixel (the pixel may change from white to black or black to white). Since it is impossible to completely eliminate the possibility of an ITL noise induced pixel error, success must be based on reducing the probability of this type of error to the point of insignificance.

The level of probability of pixel error at which pixel errors become insignificant is somewhat subjective and, for this thesis, is defined in terms of judgments made by experienced users of PtSi Infrared data [21, 22]. The idea is that if pixel errors occur at a rate of less than one-half the frame rate then, on average, there will be a pixel error in at most every other frame. In the event that the an erroneous pixel is located in a critical area of an image frame, then the frame before or after the effected frame can be used. The time between frames is 1/30 of a second, and the difference between adjacent frames is generally negligible. Using this reasoning, practical success is achieved when pixel errors occur at a rate of less than one-half the frame rate.

Given a frame rate of 30 frames per second, practical success will occur when the ITL error rate is less than 15 per second. Since there are 640 x 408 = 307,200 pixels per frame, there are $307,200 \times 30 = 9,216,000$ pixels per second. Fifteen pixel errors per second corresponds to a pixel error rate of $15/9,216,000 = 1.63 \times 10^{-6}$. If the ITL can achieve this level of performance, then it will be classified, for practical purposes, as successful.

4.9 Summary

The derivation of the absolute success criteria gives insight into the relationship between noise inherent in the signal prior to transmission and the noise that is added during the transmission process. It is interesting to note that there is a region of error performance that is dominated by noise in the signal prior to transmission. In a generalized system, this region of error performance could be exploited through clever choice of a channel encoding scheme. If channel encoding was done such that the most likely bit errors in the transmission process would be decoded at the receiver into errors that fall into the pre-transmission noise dominated region of error performance, then these errors would become insignificant and the detectable bit error rate would be reduced. In the case of the fiber optic image transmission link, this chapter has shown that a bit error rate of approximately 10^{-6} is acceptable. This figure for practical success can now be compared to the actual theoretically predicted bit error rates derived in the next chapter and the measured bit error rates documented in Chapter VI.

V. *Theoretical Performance Predictions*

Performance of the image transmission link (ITL) can be measured in terms of the bit error rate (BER), the pixel error rate, and the probability distribution of pixel error magnitudes. The objective of this chapter is to develop theoretical predictions for these performance figures and then to compare them to the success criteria determined in Chapter IV.

Analysis of the ITL circuit design (Chapter III) yields four primary error mechanisms: A/D conversion error, high-speed CMOS (H-CMOS) circuitry error, optical signal detection error, and decoding error. The A/D conversion error is classified as part of array noise (see Chapter IV), and is not included as part of the ITL noise. The total system bit error rate (BER) can be expressed, in general, as the sum of the BERs associated with each of the other three primary error mechanisms

$$P_{B(ITL)} = P_{B(H-CMOS)} + P_{B(optics)} + P_{B(decode)} \tag{16}$$

where P_B represents probability of bit error and the subscripts in parenthesis associate the probabilities with the total ITL system, the H-CMOS circuitry, optical signal detection, and decoding, respectively.

5.1 H-CMOS Circuitry Error

Buffers, latches, timing, and control circuits in the ITL are implemented using standard 74HC high-speed CMOS (H-CMOS) digital logic components. Data bits manipulated by these circuits are subject to error when noise is present on the circuit board. Noise sources in digital systems may include switching noise, thermal noise, capacitive and inductive coupling to other logic nodes, and external sources (such as power supply noise and electromagnetic signals) [30]. The total system noise tends to be additive, white, and Gaussian distributed (see Section 4.4). When the noise is of sufficient magnitude it can cause a change in logic level (from logic 0 to logic 1 or logic 1 to logic 0) and produce a bit error. The rate of errors produced in this manner depends on the noise level, the voltage thresholds between logic 0 and logic 1, and the number of bit transfers between digital components.

It has been stated that a reasonable goal for a well built digital system is to keep noise levels below 0.1 volt peak–to–peak [1, 30:7-14]. This goal can be applied to an additive, white, Gaussian noise (AWGN) model by re-stating the goal in a different form: noise deviations should be less than +/- 0.05 volts from the mean (0.1 volt peak–to–peak) 99% of the time. Using the complementary error function (see Equation 11) the standard deviation of the noise in a digital system which satisfies the re–stated goal for reasonable noise levels can be computed using the relationship

$$2Q\left(\frac{0.05}{\sigma_d}\right) = 1 - 0.99 \tag{17}$$

where σ_d is the standard deviation of the noise, and the noise is less than 0.05 volts peak–to–peak 99% of the time. Solving this equation yields $\sigma_d = 0.04$.

Voltage thresholds listed in H-CMOS manufacturer's data books [30:7-15] may be used to calculate the high and low voltage noise margins. Mathematical expressions for these noise margins are

$$M_{N(hv)} = V_{OHmin} - V_{IHmin} \tag{18}$$

and

$$M_{N(lv)} = V_{ILmax} - V_{OLmax} \tag{19}$$

where $M_{N(hv)}$ and $M_{N(lv)}$ are the high and low voltage noise margins, V_{OHmin} is the minimum output voltage for a logic high, V_{OLmax} is the maximum output voltage for logic low, V_{IHmin} is the minimum input voltage for a logic high, and V_{ILmax} is the maximum input voltage for a logic low. Noise margins have been calculated for all data interfaces in the ITL, and the worst case noise margin for a data bit transfer occurs at the interface between the 74HC174 data latch and the GA9011 HOT ROD^{TM} transmitter (see schematic diagrams in Appendix). At this interface, $V_{ILmax} = 0.8$ volts, $V_{OLmax} = 0.1$ volts, and (using Equation (19)) $M_{N(lv)} = 0.7$ volts. High and low voltage noise margins are greater at all other interfaces.

A bit error in a single transfer between logic components may occur when the noise is of greater magnitude than the noise margin of the logic components. Using the worst case noise margin of 0.7 volts, the probability of this event is calculated

(using Equation (12)) as

$$P(|\text{noise}| > +0.7) = Q\left(\frac{0.7}{\sigma_d}\right) = Q\left(\frac{0.7}{0.04}\right) \approx 7 \times 10^{-69} \tag{20}$$

The number of data bit transfers between logic components is calculated by referring to the schematic diagrams of the ITL (see Appendix). Each individual data bit is transferred 3 times in the ITL transmitter H-CMOS circuitry and 3 times in the ITL receiver H-CMOS circuitry for a total of 6 data bit transfers between logic components in the ITL.

The total probability of a data bit error due to the H-CMOS circuitry is equal to the product of the probability of a bit error in one bit transfer (from Equation 20) and the number of bit transfers. The result of this calculation yields $P_{B(H-CMOS)} \approx (7 \times 10^{-69})(6) \approx 4 \times 10^{-68}$. While this may be considered to be a rather crude approximation, it serves to illustrate the point that $P_{B(H-CMOS)}$ is extremely small and can thus be neglected.

5.2 Optical Signal Detection Error

Optical signal detection error rates depend on the optical power available at the receiver and the receiver sensitivity. The amount of optical power available in excess of the receiver sensitivity is referred to as the power margin. The power margin may be used in conjunction with receiver sensitivity specifications to calculate the expected probability of bit error in the optical portion of the ITL ($P_{B(optics)}$). The Linear Worst-Case Method is the most common method of power margin analysis. The Statistical Power Margin Method is less common, but is more accurate [4].

In the Linear Worst-Case Method of power margin analysis, manufacturer supplied worst-case specifications for each of the optical components are used to calculate the worst-case power margin. The AT&T 1252N optical transmitter and 1352N optical receiver coupled together with 0.29 NA (numerical aperture) 62.5/125 μm optical fiber have the following worst-case specifications [3]: peak optical output (transmitter) = -19 dBm, peak optical sensitivity (receiver) = -30.5 dBm @ 10^{-9} BER. These specifications are for operation at a data rate of 220 Mbits/sec. The ITL serial data rate is 250 Mbits/sec. Tests done by AT&T at bit rates above 220 Mbits/sec [5] indicate that, at ITL data rates, the transmitter optical output power

will be unchanged, while the receiver sensitivity will suffer a 1.5 dBm penalty from -30.5 dBm to -29 dBm. Worst-case losses for other system components include: 0.5 dB for high order loss (source modes that radiate from the fiber), 1.0 dB for phase-locked loop synchronization recovery circuitry, 0.8 dB for connector losses (2×0.4 dB/connector), 0.0015 dB for dispersion loss over 50 feet of optical fiber, and 0.015 dB for attenuation loss over 50 feet of optical fiber (1.0 dB/km). Using these values, the linear worst-case power margin can be calculated using

$$M_{lwc} = P_t - P_r - L_{ho} - L_{sync} - L_{conn} - L_{disp} - L_{atten} \tag{21}$$

where M_{lwc} is the linear worst-case power margin, P_t is the optical output power of the transmitter, P_r is the optical sensitivity of the receiver, L_{ho} is the high order loss, L_{sync} is the synchronization recovery loss, L_{conn} is the connector loss, L_{disp} is the dispersion loss, and L_{atten} is the optical fiber attenuation loss. Using Equation (21) the linear worst-case power margin is calculated to be $M_{lcw} = -19 - (-29) - 0.5 - 1.0 - 0.8 - 0.0015 - 0.015 \approx 7.7$ dB.

The Statistical Power Margin Method models each of the optical system power quantities as a normally-distributed random variable. The statistical power margin is calculated using the mean and variance values of each of the power quantities to calculate the mean and variance of the power margin. The mean of the power margin is defined by the equation (see Reference [4])

$$\mu_M = \mu_t - \mu_r - [\mu_c l + \mu_{co} N_{co} + \mu_D + \mu_H + \mu_{CR}] \tag{22}$$

where μ signifies the mean value, the subscripts M, t, r, c, co, D, H, and CR represent power margin, transmitter power, receiver sensitivity, cable loss, connector loss, dispersion loss, high order loss and synchronization recovery loss respectively, l is the cable length in km, and N_{co} is the number of connectors. Because the power quantities are independent, the variance of the power margin can be written as the sum of the variances (see Reference [4])

$$\sigma_M^2 = \sigma_t^2 + \sigma_r^2 + \sigma_c^2 l^2 + \sigma_{co}^2 N_{co} + \sigma_D^2 + \sigma_H^2 + \sigma_{CR}^2 \tag{23}$$

where σ^2 signifies the variance and the subscripts and other terms are defined as in Equation (22). Using Equations (22) and (23) along with specified values supplied

by AT&T [4], the mean and variance of the power margin are calculated as

$$\mu_M = -14.5 + 31.0 - [(1.0)(0.015) + (0.4)(2) + 0.0015 + 0.5 + 0.75] = 14.4 \text{ dB}$$

and

$$\sigma_M = \sqrt{(1.4)^2 + (0.7)^2 + (0.25)^2(0.015)^2 + (0.2)^2(2) + (0.3)^2 + (0)^2 + (0.25)^2} = 1.6 \text{ dB}.$$

The mean and variance of the power margin can be used to calculate the statistical power margin by specifying the 2% point of a normal distribution ($2\sigma_M$) and using the equation

$$M_{stat} = \mu_M - 2\sigma_M \tag{24}$$

where M_{stat} is the statistical power margin. Using this equation, the calculated value of M_{stat} for the ITL is $14.4 - 2(1.6) = 11.2$ dB. The interpretation of this result is that there is a 2% probability that the power margin will be less than 11.2 dB.

According to AT&T data sheets, a 1 dB increase in received optical power beyond the rated sensitivity will result in a decrease in bit error rate of approximately three orders of magnitude [4]. The receiver sensitivity used in the calculations of the linear worst-case and statistical power margins was specified for a bit error rate of 10^{-9}. Extrapolation of the BER below rated sensitivity yields expected BERs of 10^{-32} using the linear worst-case power margin or 10^{-42} using the statistical power margin. Such error rates are unlikely and virtually impossible to verify.

Documented results have verified the rule that every 1 dB in excess optical power results in a decrease in BER of three orders of magnitude at bit error rates as low as 10^{-12} [2]. It is reasonable to assume that the tremendous amount of excess received power in the ITL will result in a decrease in BER of at least three orders of magnitude beyond the verified rates of 10^{-12}. A conservative estimate, therefore, is that $P_{B(optics)} \leq 10^{-15}$.

5.3 Decoding Error

Digital data at the transmitter begins as a sequence of digitized pixel values. Each pixel is represented by a 12-bit parallel binary number. The GA9011 HOT ROD^{TM} transmitter breaks the parallel data up into 4-bit nibbles. Each 4-bit

nibble is encoded into a 5-bit code symbol using the fiber distributed data interface (FDDI) standard 4B/5B encoding shown in Table 2. Each "bit" in the code symbol is defined by the HOT ROD manufacturer as a "baud" [9]. For purposes of this thesis, however, code symbol bits will be referred to simply as code bits. Each bit of the code symbol is transmitted serially using Non-Return to Zero, Invert on ones (NRZI) format. At the receiver, the NRZI formatted code symbols are converted to NRZ, the code symbols are decoded into their original 4-bit nibbles, and the recovered data is output in a parallel format. Because of this encoding/decoding process, single code bit errors that occur due to optical signal detection error may decode into multiple bit errors in the output.

Table 2. 4B/5B Translation [9:7]

	4-BIT BINARY INPUT DATA	HEX INPUT DATA	5-BIT CODE SYMBOL OUTPUT
	0000	0	11110
	0001	1	01001
	0010	2	10100
	0011	3	10101
	0100	4	01010
	0101	5	01011
	0110	6	01110
	0111	7	01111
	1000	8	10010
	1001	9	10011
	1010	A	10110
	1011	B	10111
	1100	C	11010
	1101	D	11011
	1110	E	11100
	1111	F	11101
Sync	Idle	n/a	11111
Symbols:	Sync J	n/a	11000
	Sync K	n/a	10001

Errors that occur during the serial data transmission process in the ITL are compounded in two ways during serial data decoding at the receiver. First, single code bit errors in the NRZI formatted data are converted to sequential pairs of two

code bit errors during the NRZI to NRZ conversion process [9]. These pairs of errors may occur in the same 5-bit code symbol, or in the last bit of one code symbol and the first bit of the next. Second, code bit errors in a 5-bit NRZ code symbol may decode into an output 4–bit data nibble that is from zero to four bits different than the input data nibble.

The receiver has limited error detection and no error correction. When the GA9012 HOT ROD^{TM} receiver detects an invalid code symbol, it indicates an error condition by asserting its error line and decoding the erroneous code symbol to a 1111 data nibble on the output. Since a total of ten 4–bit data nibbles (40 bits parallel) are output simultaneously, it is possible that more than one 1111 data nibble may be output when the error line is asserted. When this happens it is impossible to determine which of the 1111 data nibbles was in error and which may be correct.

Pixels that originally consist of 12 bits (three 4-bit nibbles) are represented by 15 code bits (three 5-bit code symbols) during serial data transmission in the ITL system. Since the probability of a code bit error ($P_{B(optics)}$) in the serial NRZI data is low, it is reasonable to assume that code bit errors will be infrequent enough that the probability of more than one code bit error occurring in a given pair of pixels is negligible. This assumption translates to no more than a single pair of code bit errors in any given pair of pixels after the NRZI data is converted to NRZ. The pair of code bit errors may occur within the same pixel or as the last code bit of one pixel and the first code bit of the next.

The relationship between single code bit errors and resulting output data bit errors may be derived by considering each possible pixel code bit error condition. Each of the three 5-bit code symbols in a given pixel can represent 16 possible values. An error at a particular bit position within the code symbol may be decoded 16 different ways, depending on which of the 16 possible code symbol values was corrupted by the error. There are four possible sequential code bit pairs in a code symbol and three code symbols per pixel, giving $4 \times 3 \times 16 = 192$ possible error combinations. In addition, there are 32 possible error combinations due to single leading or trailing code bit errors (implying that the other error code bit of the pair will occur in the previous or following pixel). Finally, there are two possible code bit error pairs within the pixel that involve the trailing bit of one code symbol and leading bit of the next, for $2 \times 16 \times 16 = 512$ possible error combinations. The

total number of equally probable error combinations within one pixel is therefore $192 + 32 + 512 = 736$.

It is possible to derive the magnitude of the error caused by each of the 736 possible pixel error combinations by taking advantage of the symmetry between error combinations in each code symbol. Many of the error combinations decode to the same error magnitudes and consequently there are only 100 unique error magnitudes possible. This means that out of the 4,096 possible magnitudes represented by a 12-bit pixel, there are only 100 possible error magnitudes which may be caused by optical detection error. The probability of each error magnitude (given that an error occurred within the pixel) is given by the number of error combinations that produce a particular error magnitude divided by 736. The distribution of the relative frequencies of occurrence (out of 736 errors) of each value of error magnitude between 0 and 4,095 is plotted in Figure 8.

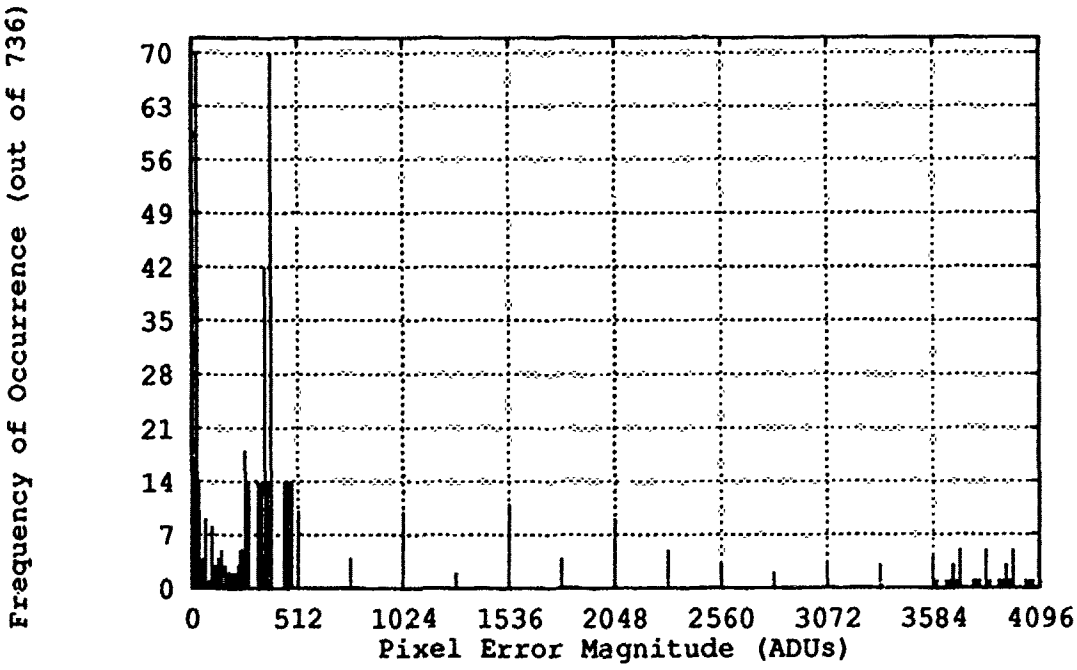


Figure 8. Frequency Distribution of Pixel Error Magnitudes

The bit error rate due to decoding is derived by considering each possible code bit error combination in relation to the number of bit errors produced in the decoded data. The cumulative total of all the data bit errors caused by each of the 736 code bit error patterns is 1,864. This means that, on average, each code bit error causes 2.53 bit errors in the output data.

5.4 *Theoretical Performance vs. Success Criteria*

The total system bit error rate, pixel error rate, and the probability distribution of error magnitudes can be written in terms of the quantities defined up to this point in Chapter V. These performance figures can then be compared to the success criteria defined in Chapter IV.

The general expression for the total system bit error rate (Equation (16)) is modified to form the more accurate expression

$$P_{B(ITL)} = P_{B(H-CMOS)} + P_{B(optics)} M_{decode} \tag{25}$$

where the expression for decoding error has been changed to the multiplying factor M_{decode} (for reasons outlined in Section 5.3). Using Equation (25) the total system bit error rate is $P_{B(ITL)} = 4 \times 10^{-68} + (10^{-15})(2.53) = 2.53 \times 10^{-15}$. This calculation shows that optical detection error is the dominant error mechanism in the ITL.

The system pixel error rate can be determined by multiplying the bit error rate by the number of bits per pixel. This calculation gives a pixel error rate of $P_{P(ITL)} = (2.53 \times 10^{-15})(12) = 3.04 \times 10^{-14}$. This rate is equivalent to an average of approximately one pixel error every 41 days.

The probability distribution of error magnitudes is determined by multiplying the frequency distribution of Figure 8 by the probability of a pixel error and dividing by the total number of possible error combinations. Performing this operation gives a distribution identical in form to that of Figure 8 but scaled in magnitude by $(3.04 \times 10^{-14})/736 = 4.13 \times 10^{-17}$. The logarithm of this probability distribution ($\log P|\text{error}_{ITL}|$), along with the logarithm of probability distribution of the detector array noise magnitudes ($\log P|\text{error}_{Array}|$) is plotted in Figure 9.

5.5 *Summary*

Theoretical performance predictions can be compared to the success criteria defined in Chapter IV using Figure 9 and the pixel error rate. It can be seen from Figure 9 that the ITL does not meet the absolute success criteria defined by Equation (15). Figure 9 also shows that the division between the detector array noise dominated region of error performance and the ITL noise dominated region of error performance occurs at $E_r = \gamma_N \approx 17$. It is interesting to note that, even with a bit

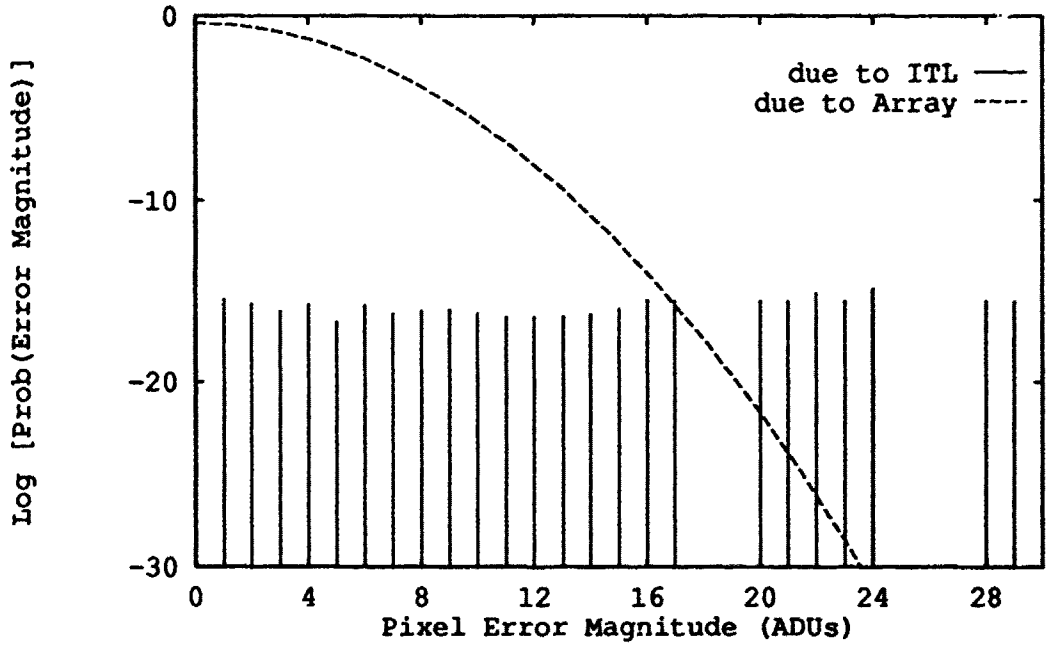


Figure 9. Probability Distribution of Pixel Error Magnitudes

error rate of 10^{-42} (as derived using the statistical power margin in Chapter IV), γ_N only increases to 28. Even though absolute success is not achieved, the predicted pixel error rate (3.04×10^{-14}) far surpasses the pixel error rate required for practical success (1.63×10^{-6}).

VI. Actual Performance Measurements

Many aspects of the actual performance of the image transmission lin. were measured for comparison to the theoretical performance predictions developed in Chapter V. The purpose of this chapter is to document the measurement methods used and to present the results of the measurements.

Design details for the ITL used in these measurements are given in Chapter III. Circuit diagrams and printed circuit board layouts are given in Appendix A and Appendix B. The measurements documented in this chapter were devised to test the following aspects of ITL performance:

1. ITL power requirements
2. Bit and pixel error rates
3. Sensitivity to sample clock duty cycle variations
4. Maximum pixel transmission rate
5. Sensitivity of minimum pixel transmission rate to heating
6. Installation in the Infrared camera

Measurements involving each of these aspects of ITL performance are documented separately.

6.1 ITL Power Requirements

Power requirements for the ITL transmitter and receiver boards were measured separately using a Tektronix DM501A digital ammeter in series with the +5 volt, +15 volt, and -5.2 volt power supplies. Measurements were performed while the ITL was running at the full serial bit rate of 250 Mbits/second Results were as follows:

1. Transmitter +5 volt supply: 0.994 Amperes
2. Transmitter -5.2 volt supply: 0.419 Amperes
3. Transmitter +15 volt supply: 0.0198 Amperes
4. Receiver +5 volt supply: 0.736 Amperes

6.2 Bit and Pixel Error Rates

Bit and pixel error rates were measured using a custom built test circuit. A schematic diagram of the test circuit is included in the Appendix C. A brief discussion of the test circuit is included in this section, followed by the results of the tests.

6.2.1 The Error Rate Test Circuit The error rate test circuit may be broken down into two parts: the transmitter sequence generator, and the receiver sequence comparator. Both parts of the test circuit were constructed on a single wire-wrapped circuit board using low power Schottky transistor-transistor logic (LSTTL) devices. A block diagram of the error rate test circuit is given in Figure 10.

The transmitter sequence generator is connected in place of the analog-to-digital (A/D) converter on the ITL transmitter board. It consists of a 12-bit counter and a pixel sample clock simulation circuit. A single DIP switch is used to clear the 12-bit counter and inhibit the simulated pixel sample clock. The simulated pixel sample clock was created using a Wavetek model 148 function generator set to generate TTL level square waves. The simulated pixel sample clock is connected to the SAMPLE IN input on the ITL transmitter board. The A/D converter was removed from the ITL transmitter board, and the 12-bit output of the counter was connected to the A/D converter socket in place of the 12 A/D converter outputs. The SAMPLE pin on the A/D converter socket was used to clock the 12-bit counter.

The receiver sequence comparator is connected to the output of the ITL receiver board, where it compares the received 12-bit sequence to an independently generated copy of the sequence. The receiver sequence comparator consists of a data latch, a 12-bit counter, a 12-bit comparator, a 4-bit error counter, and various light emitting diodes (LEDs). The data latch is used to latch in the received data and hold it for comparison to the output of the 12-bit counter. The 12-bit counter counts on the pixel clock output from the ITL receiver board and is identical to the counter used in the transmitter sequence generator. The 12-bit comparator is used to compare the outputs from the data latch and the 12-bit counter. The output from the 12-bit comparator is asserted whenever any of the 12 bits from the counter do not match with the 12 bits from the data latch. The comparator output is connected to a the 4-bit error counter. The 4-bit error counter counts the number of times an error is indicated by the 12-bit comparator. LEDs are used visually indicate the number of errors accumulated by the 4-bit counter.

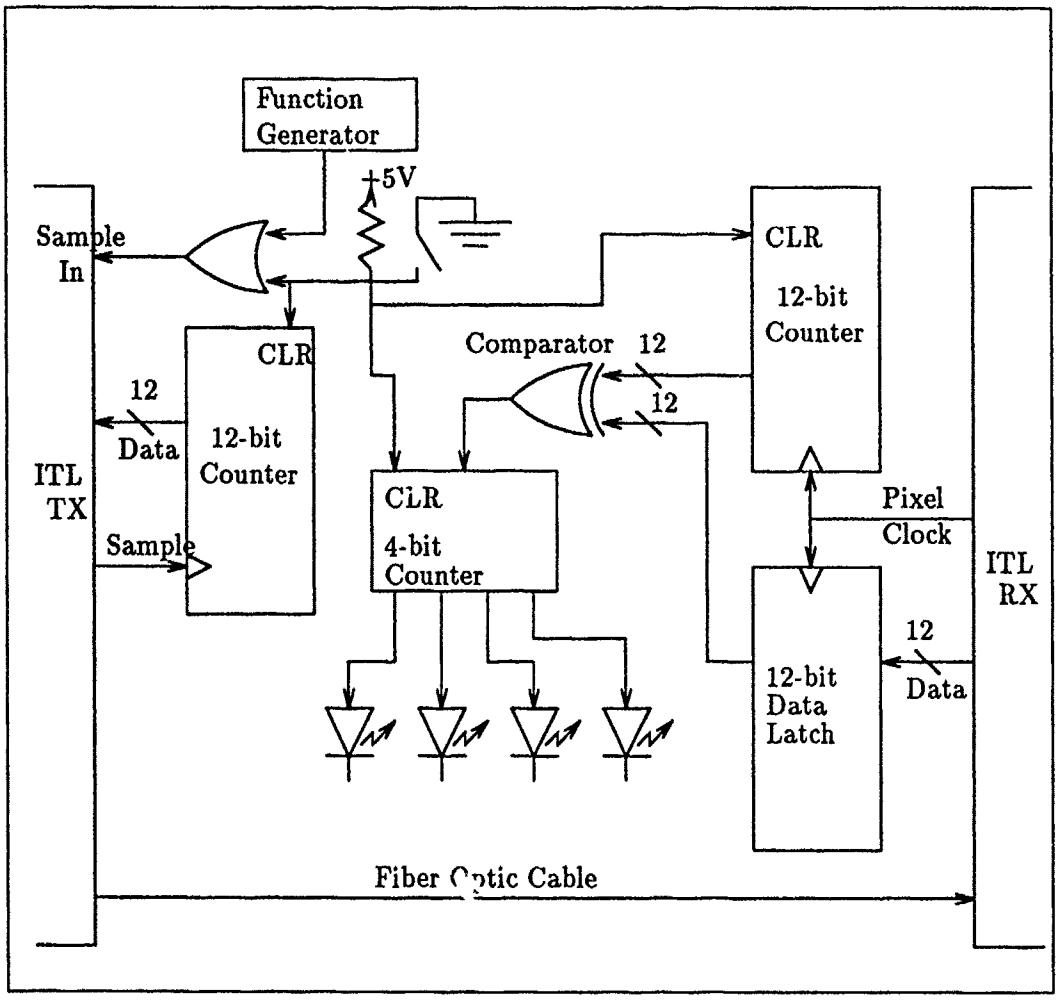


Figure 10. The Error Rate Test Circuit

In operation, the transmitter sequence generator generates a repeating 12-bit sequence that starts at 0000 0000 0000 and counts up to 1111 1111 1111. This sequence includes all 4,096 possible 12-bit combinations. The sequence of simulated pixels is inserted into the ITL transmitted board at the point where the output of the A/D converter would normally insert digitized pixel values. The ITL transmitter board then transmits the repeating sequence over the optical fiber to the receiver board. The receiver sequence comparator is connected to the output of the receiver board. The pixel clock output from the receiver board indicates that new data is ready. This pixel clock signal is used as the count input to the 12-bit counter in the receiver sequence comparator. The actual data at the output of the receiver board

is compared bit by bit to the output of the 12-bit counter. If the comparator detects a difference, then the output is asserted to indicate an error has occurred. Error indications are accumulated and displayed in binary format on a set of four LEDs.

6.2.2 Error Rate Test Results Error rates were measured at four different transmission rates in order to simulate pixel transmission rates used by actual Platinum Silicide (PtSi) Focal Plane Array (FPA) cameras. Pixel transmission rates tested include: 9.5×10^6 pixels/second, 3.2×10^6 pixels/second, 1.6×10^6 pixels/second, and 1.0×10^3 pixels per second. All error rate tests (except as noted below) were conducted using manufacturer provided heat sinks and 3 inch diameter 110 Volt/0.8 Amp muffin fans for cooling on the GA9011 and GA9012 HOT ROD^{TM} chips (heating considerations are discussed in detail in Section 6.5).

At 9.5×10^6 pixels per second the ITL is approaching the designed maximum speed of 10^7 pixels/second. This rate also approaches the projected pixel rates of future high resolution (640 x 480) PtSi cameras. At this pixel rate the ITL was run for 30.75 hours, resulting in the transmission of 1.13×10^{13} data bits (1.05×10^{12} pixels). No errors were recorded. The bit error rate (BER) is thus less than 10^{-13} (pixel error rate $< 10^{-12}$).

Existing 320 x 244 PtSi cameras run at 3.2×10^6 pixels per second. The ITL was run at this rate for 8.6 hours using the error rate test circuit. In this time period, 1.2×10^{12} data bits (10^{11} pixels) were transmitted with no errors recorded. This corresponds to a BER of less than 10^{-12} (pixel error rate $< 10^{-11}$).

The most commonly used PtSi camera is currently the 160 x 244 pixel camera, which runs at 1.6×10^6 pixels per second. The ITL was run at this rate for 22.2 hours using the error rate test circuit. In this time period, 1.5×10^{12} data bits (1.3×10^{11} pixels) were transmitted with no errors recorded. This corresponds to a BER of less than 10^{-12} (pixel error rate $< 10^{-11}$).

The blanking time (time period with no active pixels) in the 160 x 244 pixel camera is on the order of 10^{-3} seconds. The ITL was run at 1.0×10^3 pixels per second to simulate these long blanking times. In order to simulate probable heating conditions in the eventual camera installation, this test was performed using heat sinks (but no fans) on the GA9011/GA9012 HOT ROD^{TM} chips (heating considerations and reasoning behind this configuration are discussed in Section 6.5). In this configuration, the test was run for 17 minutes with no errors recorded. In this time

period, over 10^7 data bits (10^6 pixels) were transmitted with no errors recorded. The corresponding BER is less than 10^{-7} (pixel error rate $< 10^{-6}$).

6.3 Sensitivity to Sample Clock Duty Cycle Variations

The manufacturer of the DDU-224F-200 digital delay unit (used on the ITL transmitter board) indicates that problems may occur with this unit when the pulse width/delay time ratio is less than one [6]. While the manufacturer's suggestions for eliminating these problems were considered during design of the ITL, some concern remained. This section documents tests conducted to determine sensitivity of the ITL to variations in the sample clock pulse configuration.

The ITL test configuration used was exactly the same as that used in the error rate tests. The duty cycle of the simulated pixel sample clock was varied using controls on the function generator. The ITL was tested at pixel rates of 1.0, 2.2, and 9.1 Mpixels per second. The error rate test circuit showed no errors at any of these pixel rates as long as the duty cycle was held between 5% and 95%. When the duty cycle exceeded these limits, the ITL lost synchronization and errors were displayed continuously.

It should be noted that in order to use the error rate test circuit, the A/D converter was removed. Specifications for the A/D converter [31] indicate that it requires a pixel sample clock duty cycle of between 30% and 70% at sample rates approaching 10^7 samples per second. The A/D converter will thus be the limiting factor in duty cycle specifications.

6.4 Maximum Pixel Transmission Rate

The designed maximum pixel transmission rate is 10 Mpixels per second. The actual maximum was tested by using the error rate test circuit (configured exactly as in the error rate tests) and increasing the frequency of the simulated pixel sample clock until errors were indicated. The measured maximum pixel transmission rate was 9.96 Mpixels per second. The test was repeated with and without fans and heat sinks, but no changes in the results were noted.

6.5 Sensitivity of Minimum Pixel Transmission Rate to Heating

The manufacturer of the GA9011 and GA9012 HOT ROD^{TM} chip set has noted a "first word corruption" problem with the devices when operating at low

data rates [10][11]. The first word corruption problem occurs in the first transmitted data word after the system has been idle for a period of time. In this situation, the received data word is corrupted. The problem has been noted to be especially acute as the GA9011 and GA9012 heat up due to normal operational heat dissipation. The manufacturer recommends a combination of heat sinks and forced air flow to reduce the problem.

The ITL is designed to be included as an integral part of an infrared camera system. In such a system, the ITL transmitter board would be mounted with other camera electronics inside the camera chassis. The camera chassis does not include any form of cooling air circulation. Forced air circulation is provided in the image processor chassis in which the ITL receiver board will be mounted. The purpose of the tests documented in this section is to determine the extent of the first word corruption problem in the ITL.

Tests were conducted to determine the minimum pixel rate at which the ITL would operate under various different cooling configurations. No attempt was made to measure actual chip temperatures, but only to test under differing conditions in order to get a general idea of the extent of the problem. The error rate test circuit was used to monitor errors as the pixel transmission rate was slowly decreased. Cooling fans and heat sinks applied to the GA9012 receiver chip under various conditions provided no noticible change in operating characteristics of the ITL, while cooling configuration changes to the GA9011 transmitter chip caused dramatic changes.

The cooling devices used were heat sinks provided by the GA9011/GA9012 manufacturer, and three inch diameter "muffin" fans. The heat sinks measured approximately 0.6 x 0.6 x 0.4 inches and were made of a black metallic material. The heat sinks were intended to be attached to the chips with thermally conductive epoxy [11], but, for ease of removal, these tests were conducted with the heat sinks sitting on top of the chips with gravity as the only means of attachment (to allow easy removal of the heat sinks during testing). The fans used were 3 inch diameter 110 volt 0.8 amp "muffin" fans of the type commonly used to circulate air through personal computer chassis.

With heat sinks and fans, the ITL pixel rate was slowly reduced until bit errors began to be indicated on error rate test circuit LEDs. This occurred at approximately 50 pixels per second. At 50 pixels per second, bit errors were recorded at a rate of approximately one error every ten seconds.

With heat sinks only (no fans), the experiment was repeated. No errors were indicated until the pixel rate was reduced to 500 pixels per second. At 500 pixels per second the error rate was approximately one bit error every three seconds.

With no fans or heat sinks the experiment was again repeated. No errors were indicated until the pixel rate was reduced to 3,700 pixels per second. At 3,700 pixels per second the error rate was approximately one bit error every three seconds.

The longest time between data transmissions in the ITL is likely to be during the vertical blanking time in the 160 x 244 pixel IR camera. This blanking time is 588 μs. The frequency of a periodic signal with a period of 588 μs is 1.7 KHz. Using this reasoning, it was decided that 1.0 Kpixels per second would be a good lower bound on expected pixel rates.

From a cold start, the ITL was run at 1.0 Kpixels per second with no heat sinks or fans. Initially no errors were recorded. At approximately three minutes from turn-on, errors began to be indicated at about one error per second. At five minutes from turn-on the error rate had increased to about three bit errors per second, and by 30 minutes from turn-on the rate stabilized to approximately 20 errors per second. When the heat sink and fan were applied, the error rate dropped within one second and no errors were recorded for five minutes. The heat sink was then removed (leaving the fan) and the error rate stabilized to about one bit error per minute after 20 minutes. When the fan was removed the error rate increased, but replacing the heat sink (with no fan) caused the error rate to drop again almost immediately and no errors were recorded for the next 17 minutes.

6.6 Installation in the Infrared Camera

The ITL was installed on a 160 x 244 PtSi FPA camera owned by the Geophysics Directorate of the Phillips Laboratory (PL/GD). The installation was accomplished at PL/GD facilities at Hanscom AFB, Massachusetts. Data transmitted by the ITL was displayed on a MaxVideo^{TM} image processor built by DataCube, Inc. The pixel rate for this camera is 1.6 Mpixels per second. Figures 11 and 12 are infrared images that were transmitted by the ITL in this configuration.

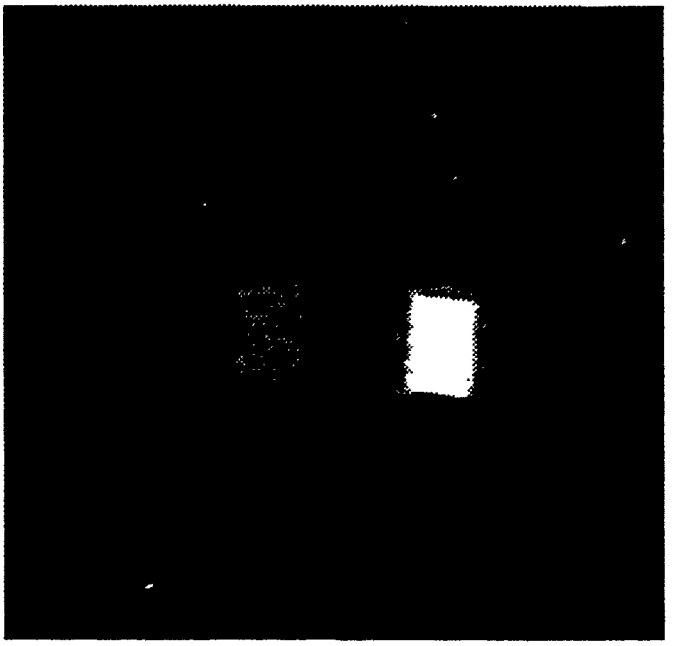


Figure 11. 160 x 244 PtSi IR image of an IR calibration source transmitted using the ITL

Figure 12. 160 x 244 PtSi IR image of a face transmitted using the ITL

6.7 Summary

Test results show that the image transmission link exceeds the minimum levels required for success. Actual installation in a 160 x 244 PtSi infrared camera proves that the the ITL is capable of transmitting medium resolution imagery as an integral part of the camera system. Bit error rate tests at bit rates approaching the requirements of the 640 x 480 PtSi infrared cameras show that the ITL should perform equally well when high resolution cameras become available for testing.

VII. Conclusions and Recommendations

This thesis has presented a design for a fiber optic image transmission link (ITL) that meets the requirements for inclusion as an integral part of an infrared camera system. The ITL helps to solve the fundamental problem of aircraft noise in airborne infrared imagery. As a secondary benefit, the ITL provides an interface between a variety of infrared camera systems and a commercially available image processor. This chapter provides conclusions based on the results obtained in the thesis, along with recommendations for related work in the future.

7.1 Summary

Chapter I listed four research objectives: 1) present an original design for a fiber optic image transmission link capable of transmitting 640 x 480 pixel images, 2) establish criteria for determining the success or failure of the image transmission link, 3) mathematically model the design to predict its performance, and 4) verify theoretical predictions through actual measurements. Chapter III presented the design for the image transmission link, satisfying the first research objective. The second and third research objectives were covered in Chapter IV and Chapter V, respectively. Finally, the fourth research objective was treated in Chapter VI.

7.2 Conclusions

The criteria determined for practical success in Chapter IV suggest that the ITL can be classified as a success if the BER is better than 1.63×10^{-6}. Bit error rate (BER) measurements documented in Chapter VI show that the BER of the ITL has an upper bound of 10^{-13} (no errors in 10^{13} transmitted bits), and the predicted BER (from Chapter V) was better than 10^{-15}. Clearly the error rate performance of the ITL can be classified as successful.

Infrared images transmitted by the ITL (see Chapter VI) prove that it is capable of performing its designed function with medium resolution images (160 x 244 pixels) in a laboratory environment. A true test of the ITL capabilities will be transmission of high resolution images (640 x 480 pixels) in an aircraft environment. Successful bit error rate tests at bit rates required for high resolution image transmission (see Chapter VI) indicate that the ITL is capable of the speed necessary for

transmitting the high resolution images, but operational 640 x 480 IR cameras are net yet available for ITL testing with actual high resolution imagery.

7.3 Recommendations for Future Research

Future research involving the fiber optic image transmission link should focus on two primary areas: transmission of high resolution images and flight testing. Tests involving the ability of the ITL to transmit high resolution images will have to wait until working high resolution IR cameras become available. Flight testing, however, involves many aspects that can be tested immediately.

A significant theoretical result from Chapter IV also calls for further investigation. This is the idea that, through a clever choice of a channel encoding scheme, bit errors that occur during the transmission process can be decoded into a region of error performance dominated by noise inherent in the signal prior to transmission. If channel encoding is done such that the most likely bit errors in the transmission process would be decoded at the receiver into errors that fall into the pre-transmission noise dominated region of error performance, then these errors would become insignificant compared to the signal noise and the detectable bit error rate would be reduced. This idea could be exploited by any digital data transmission system in which the signal to be transmitted has some finite amount of noise associated with it prior to transmission (for example audio and video type signals). The implementation of this idea could be compared to pre-emphasis and de-emphasis techniques used for years in the transmission of analog signals to reduce the effect of noise introduced during the transmission process.

Appendix A. *ITL Transmitter Board Schematics and PC Layouts*

143

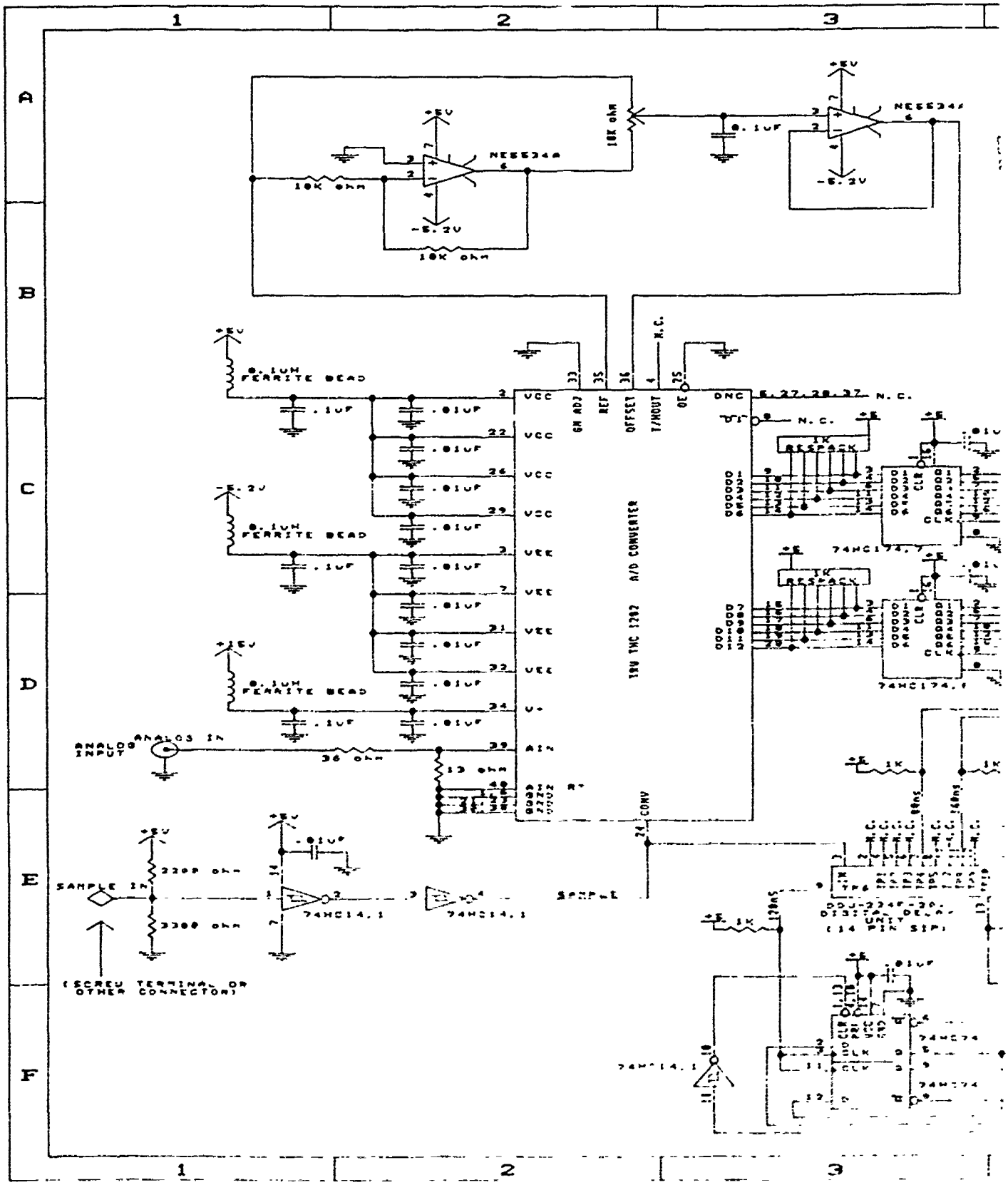
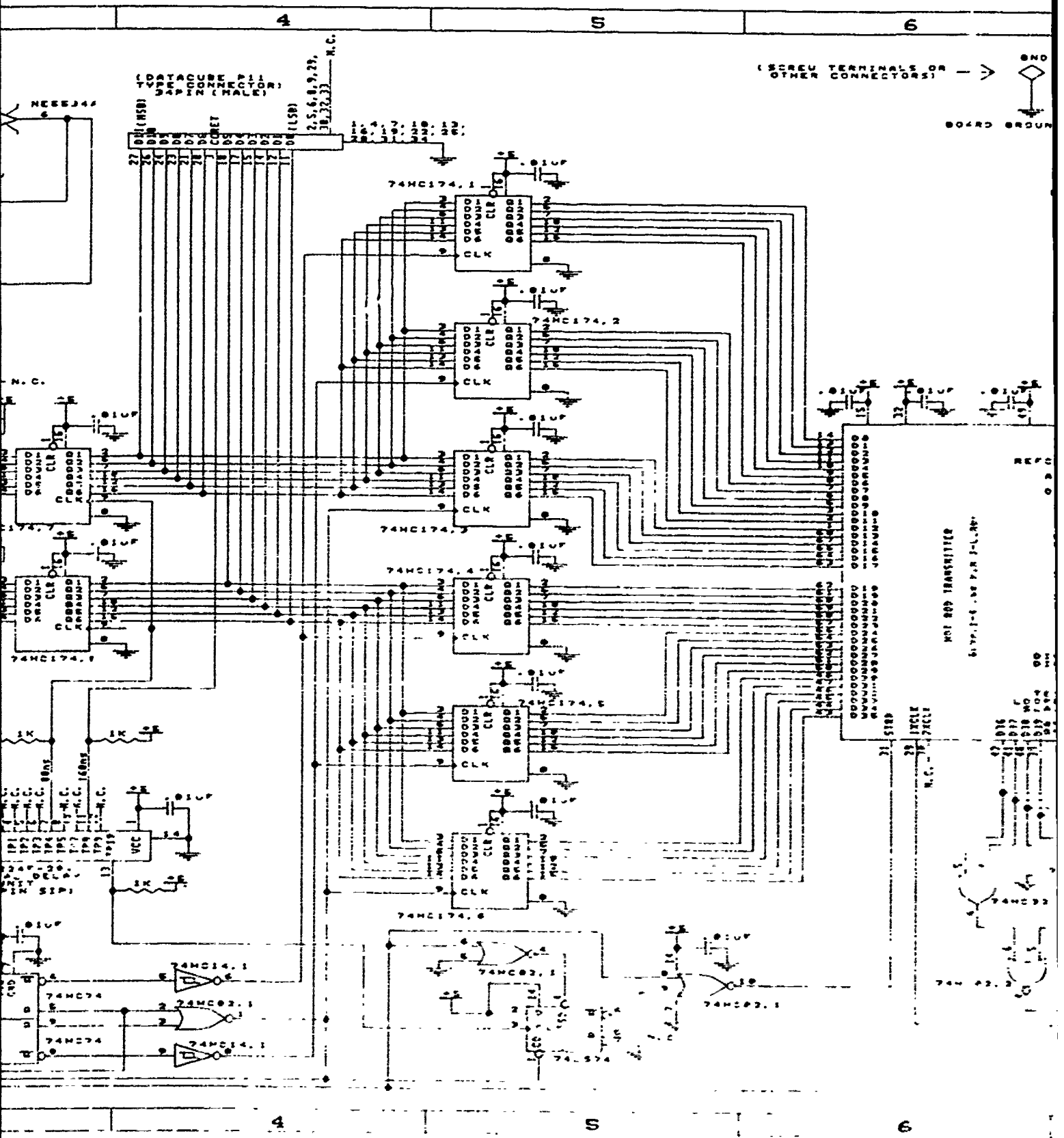
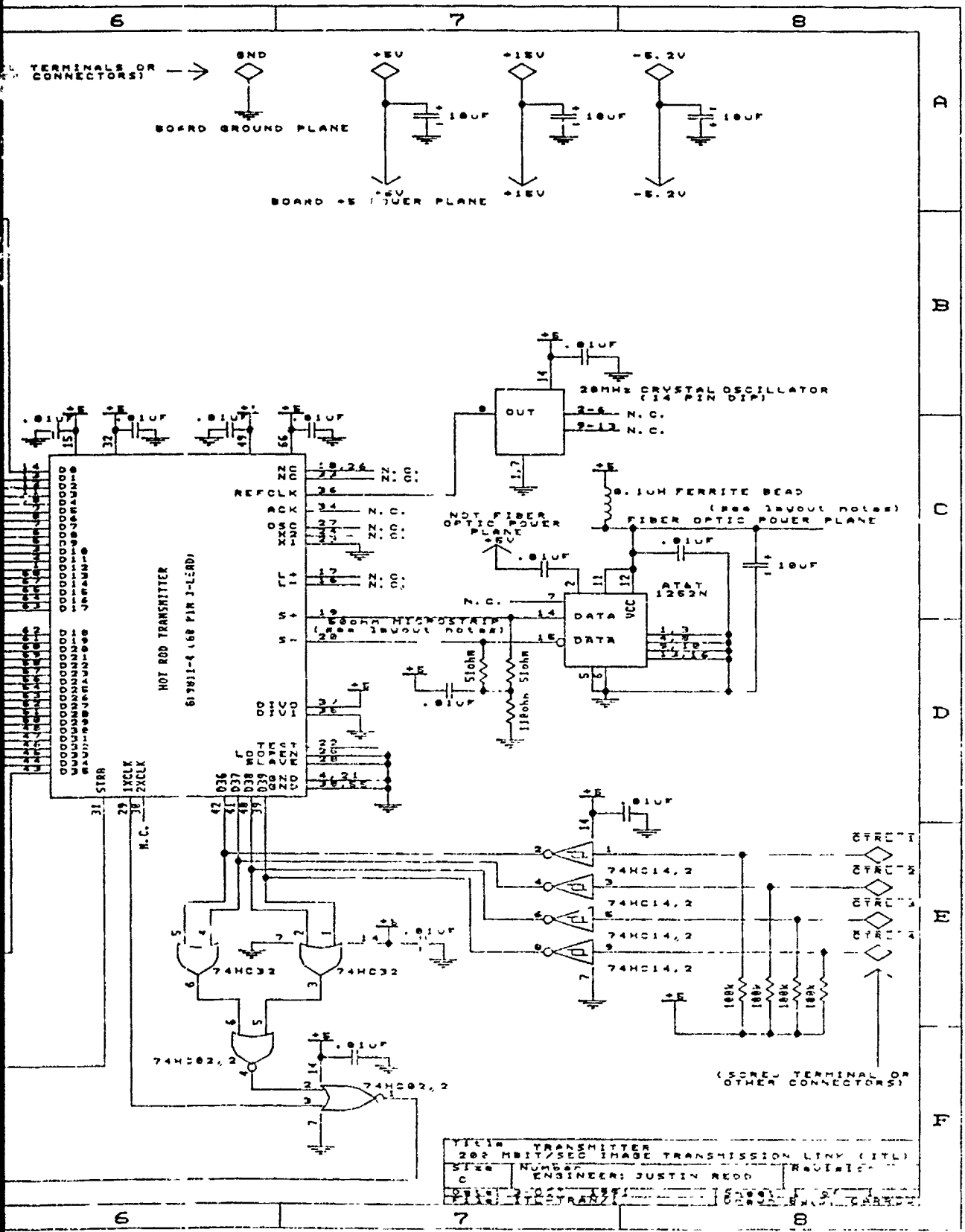


Figure 13. ITL Transmitter Board - Schematics

2 of 3


4
5
6
74HC174.1
74HC174.2
74HC174.3
74HC174.4
74HC174.5
74HC174.6
74HC14.1
74HC74
74HC02.1
1K
.01UF
VCC
GND
BOARD GROUND
(SCREW TERMINALS OR OTHER CONNECTORS)
(DATACUBE PII TYPE RIBBON CONNECTOR) 34 PIN (MALE)
N.C.


6
7
8
A
B
C
D
E
F
TERMINALS OR CONNECTORS)
GND
+5V
+15V
-5.2V
10UF
BOARD GROUND PLANE
BOARD +5 POWER PLANE
.01UF
20MHz CRYSTAL OSCILLATOR (14 PIN DIP)
OUT
N.C.
HOT ROD TRANSMITTER
REFCLK
ACK
N.C.
STRB
1XCLK
2XCLK
N.C.
2.2UH FERRITE BEAD
(FOR INVOUT NOISE)
NOT FIBER OPTIC POWER PLANE
FIBER OPTIC POWER PLANE
ATAT 1262N
DATA
VCC
510ohm
110ohm
74HC14,2
74HC32
74HC02,2
100K
(SCREW TERMINAL OR OTHER CONNECTORS)
TITLE: TRANSMITTER
200 MBIT/SEC IMAGE TRANSMISSION LINK (ITL)
SIZE
C
NUMBER
ENGINEER: JUSTIN REDD
REVISION

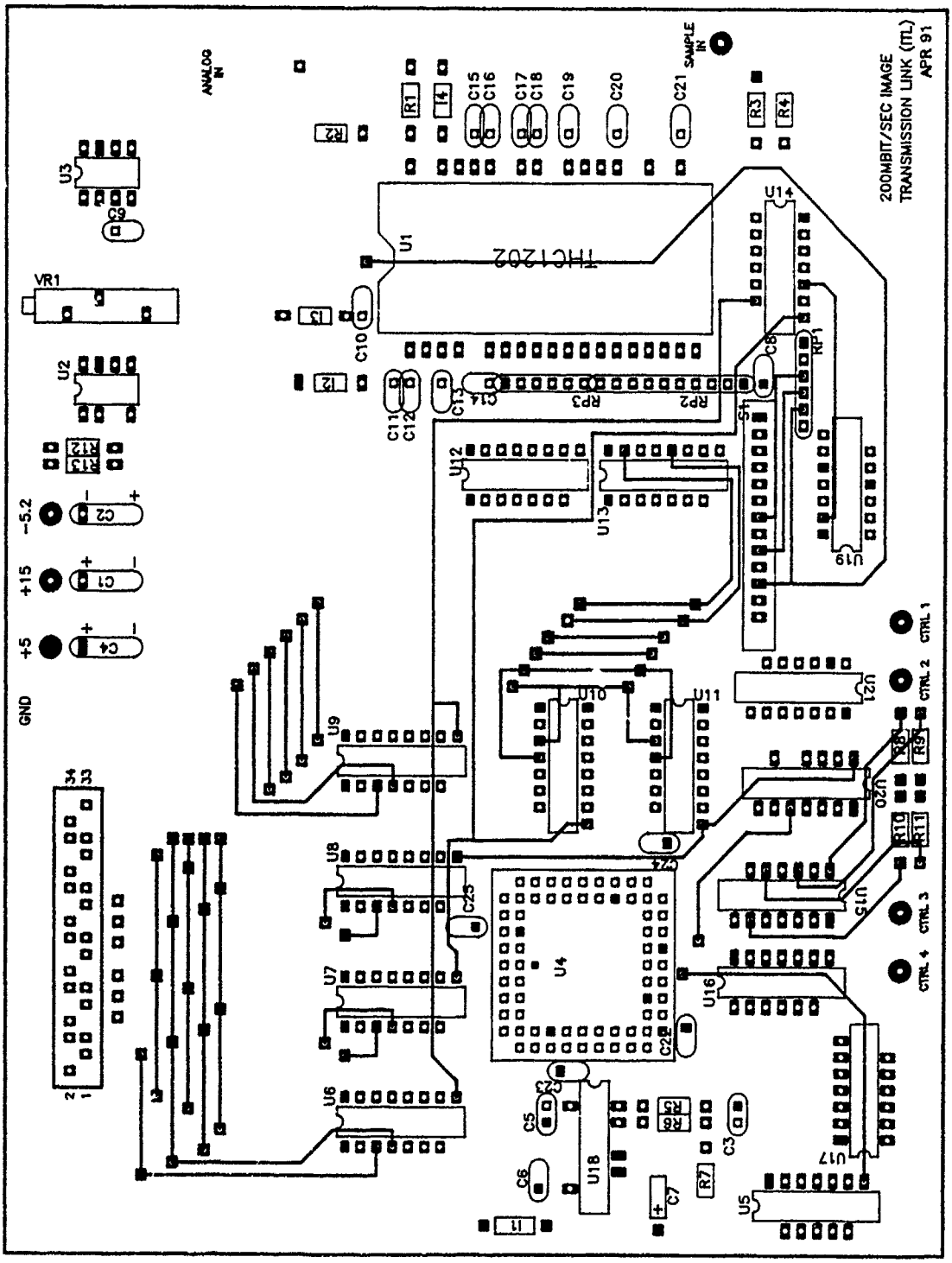


Figure 14. ITL Transmitter Board - PC Board Layout (TOP)

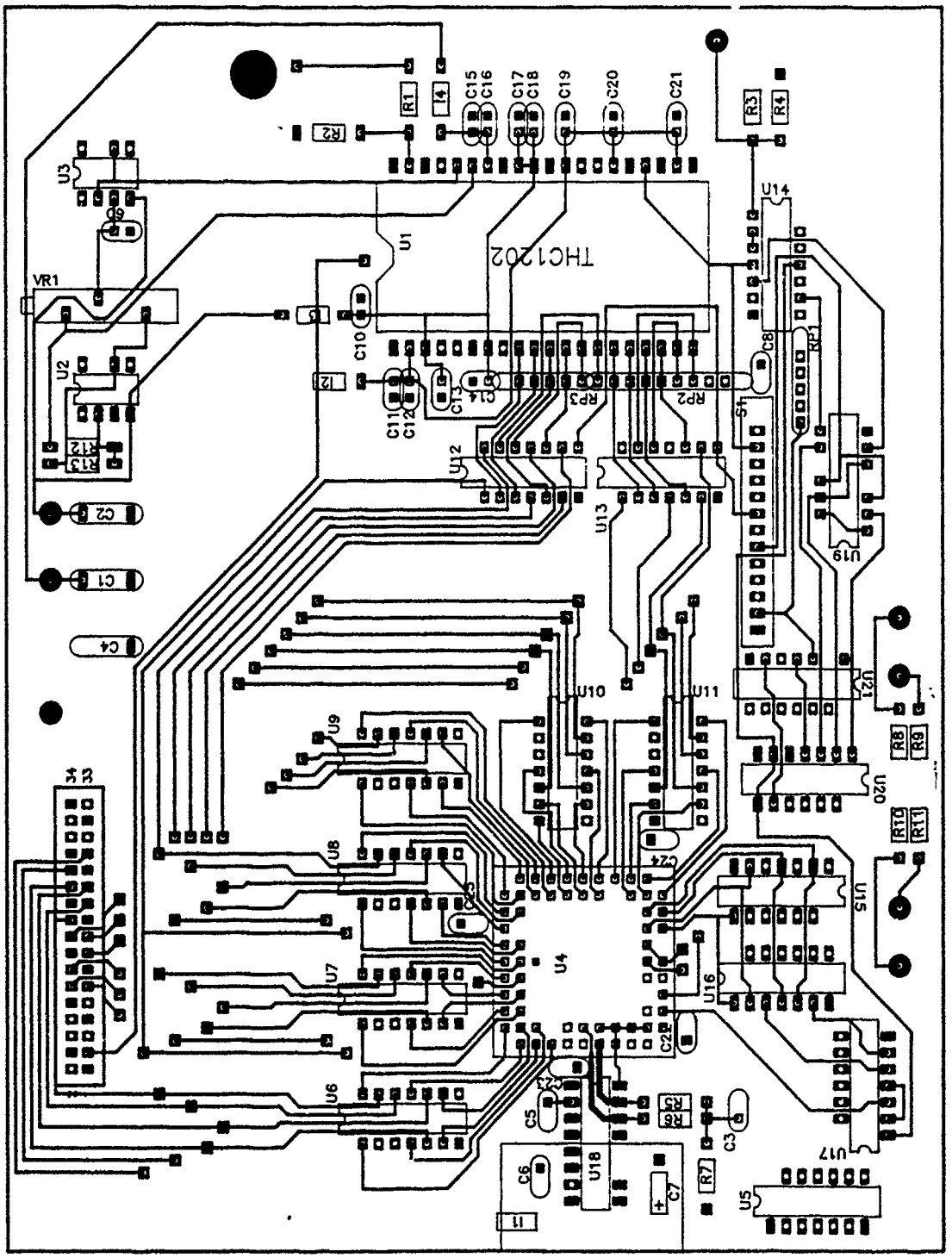


Figure 15. ITL Transmitter Board - PC Board Layout (BOTTOM)

Bill of Materials ITL-TRAN.PCB

200MBIT/SEC ITL

Quantity	Type	Value	Ref Designators
6	.1uF	.1uF	C3,C5,C6,C8,C9,C10
15	.01uF	.01uF	C11,C12,C13,C14,C15,C16, C17,C18,C19,C20,C21,C22, C23,C24,C25
4	.1uH	0.1uH	I1,I2,I3,I4
3	1K	1K	RP1,RP2,RP3
1	2.2K	2.2Kohms	R3
1	3.3K	3.3Kohm	R4
2	10K	10Kohm	R12,R13
1	10k	10K	VR1
4	10uF	10uF	C1,C2,C4,C7
1	13ohm	13ohm	R2
1	20MHz CRYSTAL	20MHz CRYSTAL	U5
1	36ohm	36ohm	R1
2	51ohm	51ohm	R5,R6
1	74HC02,1	74HC02,1	U20
1	74HC02,2	74HC02,2	U17
1	74HC14,1	74HC14,1	U14
1	74HC14,2	74HC14,2	U15
1	74HC32	74HC32	U16
1	74HC74	74HC74	U19
1	74HC74,2	74HC74,2	U21
1	74HC174,1	74HC174,1	U6
1	74HC174,2	74HC174,2	U7
1	74HC174,3	74HC174,3	U8
1	74HC174,4	74HC174,4	U9
1	74HC174,5	74HC174,5	U10
1	74HC174,6	74HC174,6	U11
1	74HC174,7	74HC174,7	U12
1	74HC174,8	74HC174,8	U13
4	100K	100Kohm	R8,R9,R10,R11
1	110ohm	110ohm	R7
1	1252N	AT&T 1252N	U18
1	DDU-224F-200	DDU-224F-200	S1
1	GA9011	GA9011	U4
1	NE5534A,1	NE5534A,1	U2
1	NE5534A,2	NE5534A,2	U3
1	THC1202	A/D CONVERTER	U1

Appendix B. *ITL Receiver Board Schematics and PC Layouts*

1 of 3

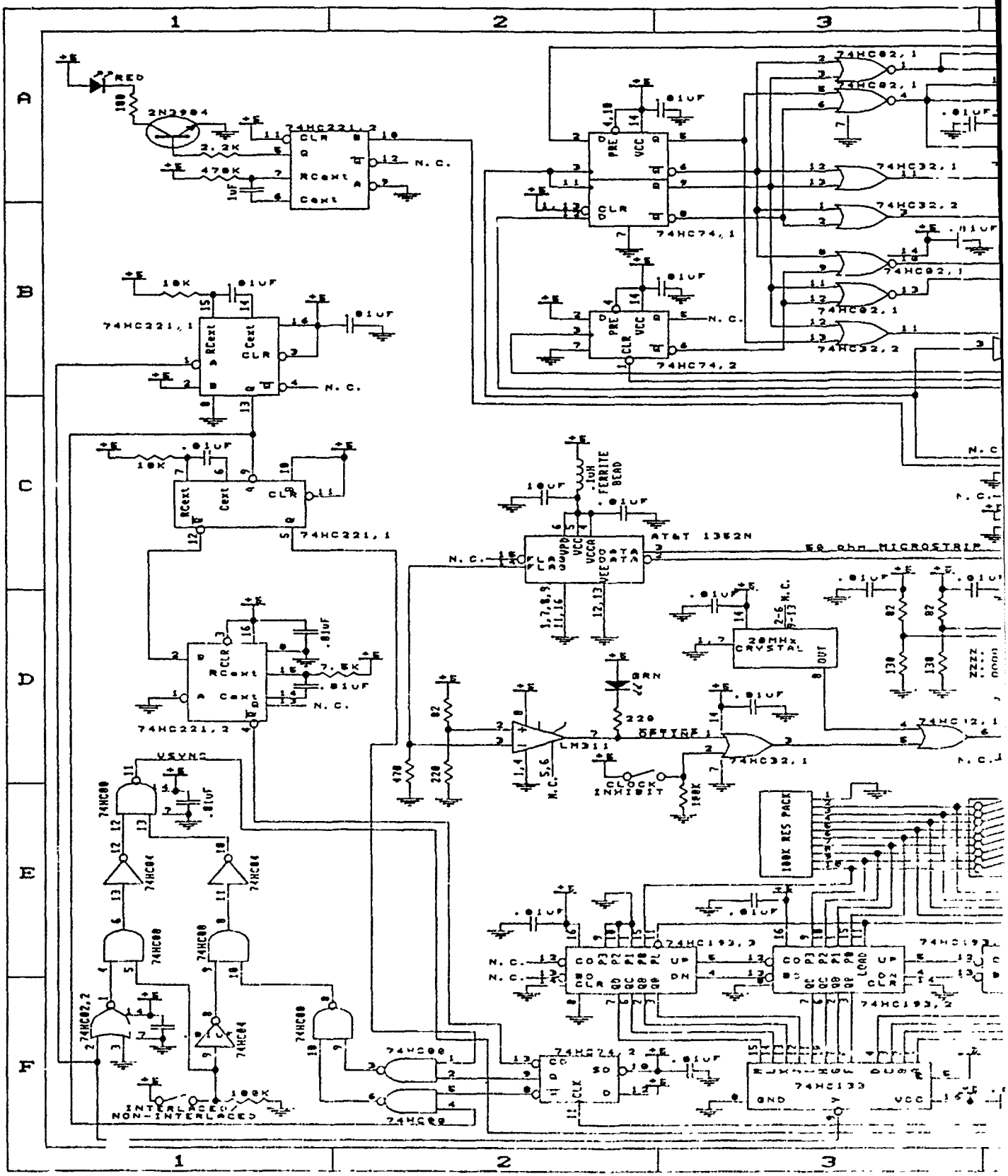
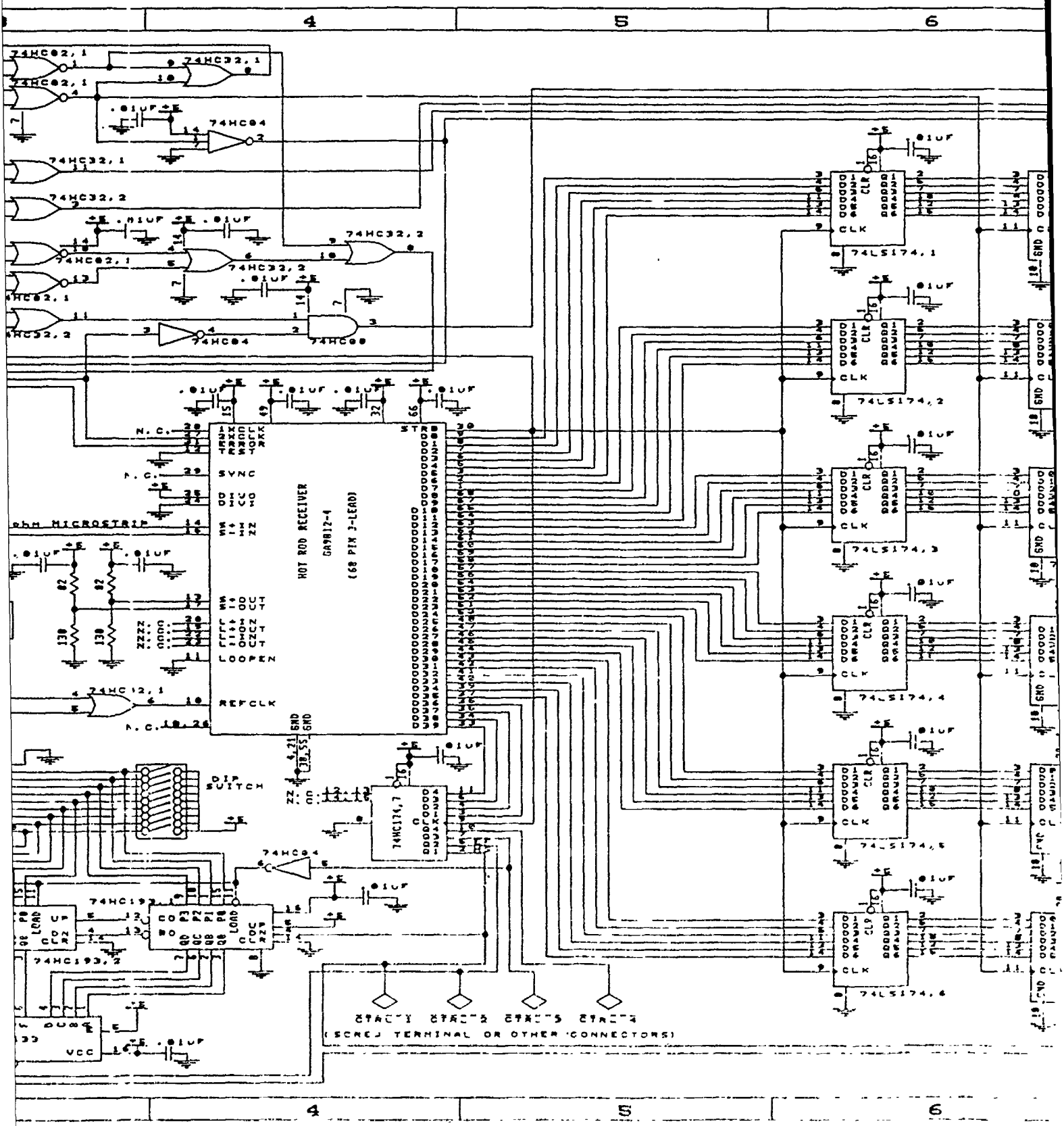
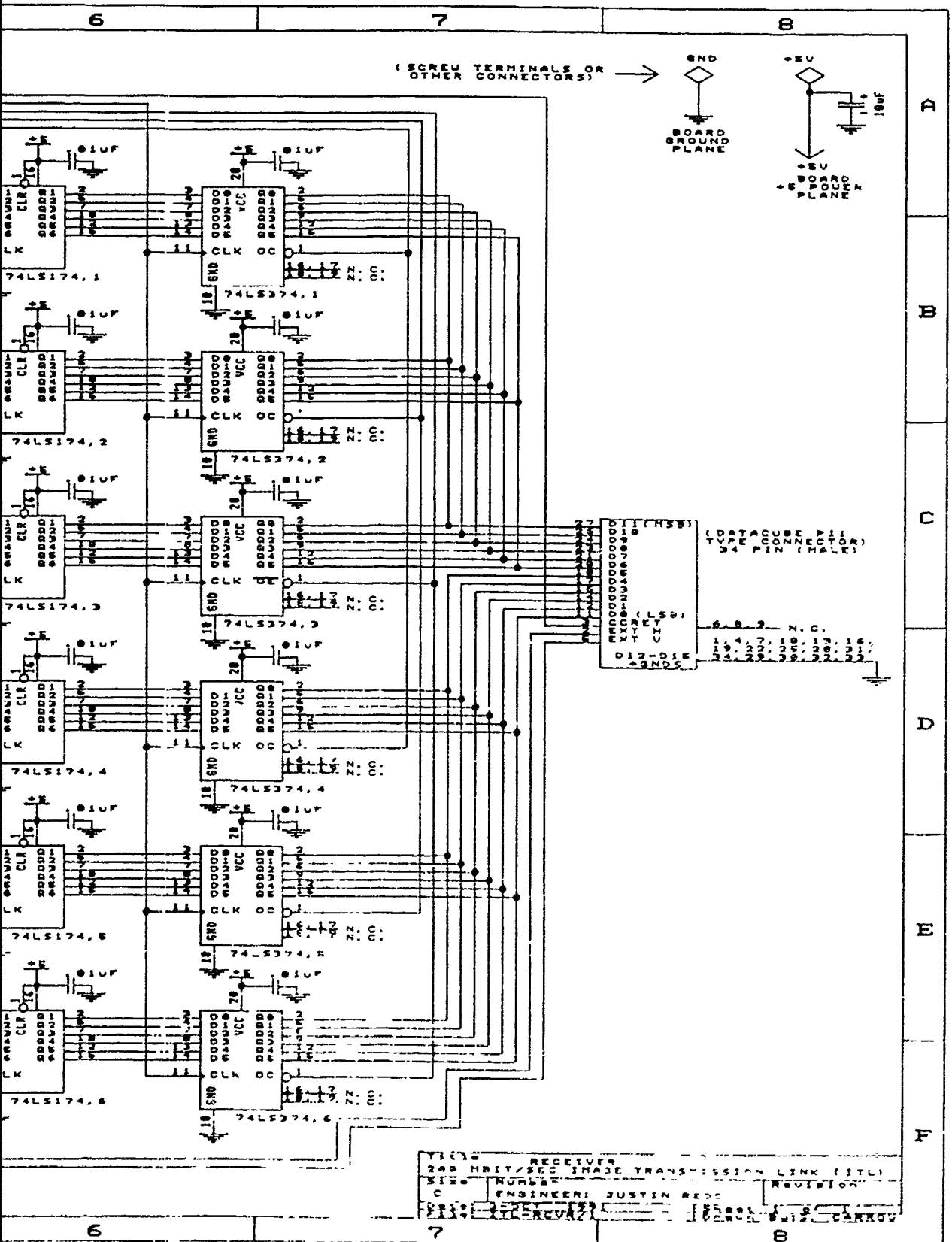


Figure 16. ITL Receiver Board - Schematics

2 of 3


4
5
6
HOT ROD RECEIVER
GA9812-4
(68 PIN J-LEAD)
74HC02, 1
74HC32, 1
74HC32, 2
74HC04
74HC08
74HC12, 1
74HC174, 1
74HC193, 2
74LS174, 1
74LS174, 2
74LS174, 3
74LS174, 4
74LS174, 5
74LS174, 6
.01UF
82
130
ohm MICROSTRIP
DIP SWITCH
SYNC
LOOPEN
REFCLK
N.C.
VCC
(SCREW TERMINAL OR OTHER CONNECTORS)


6
7
8
A
B
C
D
E
F
(SCREW TERMINALS OR OTHER CONNECTORS)
GND
BOARD GROUND PLANE
+5V
+5V BOARD +5 POWER PLANE
.1UF
74LS174,1
74LS374,1
74LS174,2
74LS374,2
74LS174,3
74LS374,3
74LS174,4
74LS374,4
74LS174,5
74LS374,5
74LS174,6
74LS374,6
(DATACUBE PII TYPE CONNECTOR) 34 PIN (MALE)
D12-D15 +5VDS
RECEIVER
200 MBIT/SEC IMAGE TRANSMISSION LINK (ITL)
ENGINEER: JUSTIN REED

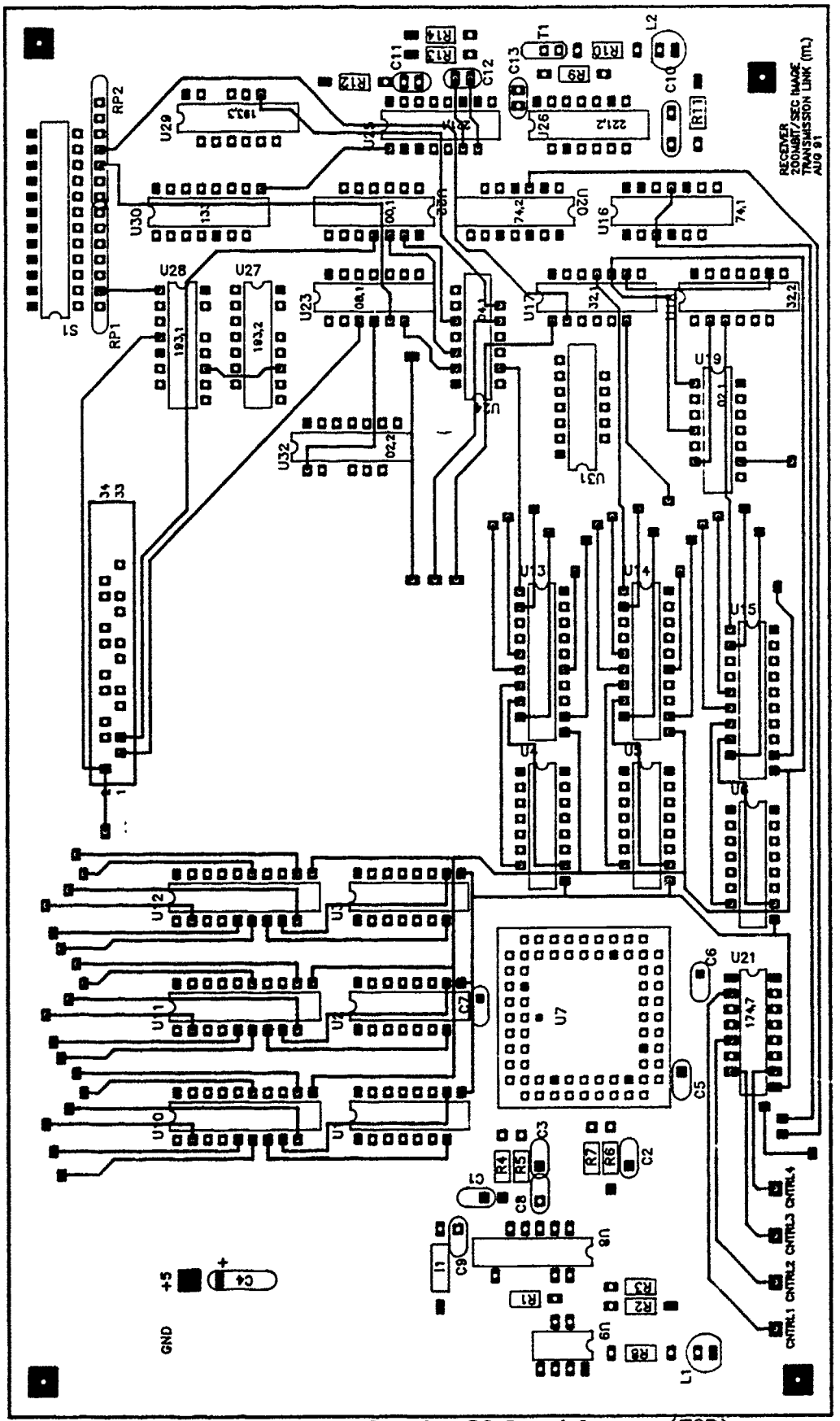


Figure 17. ITL Receiver Board - PC Board Layout (TOP)

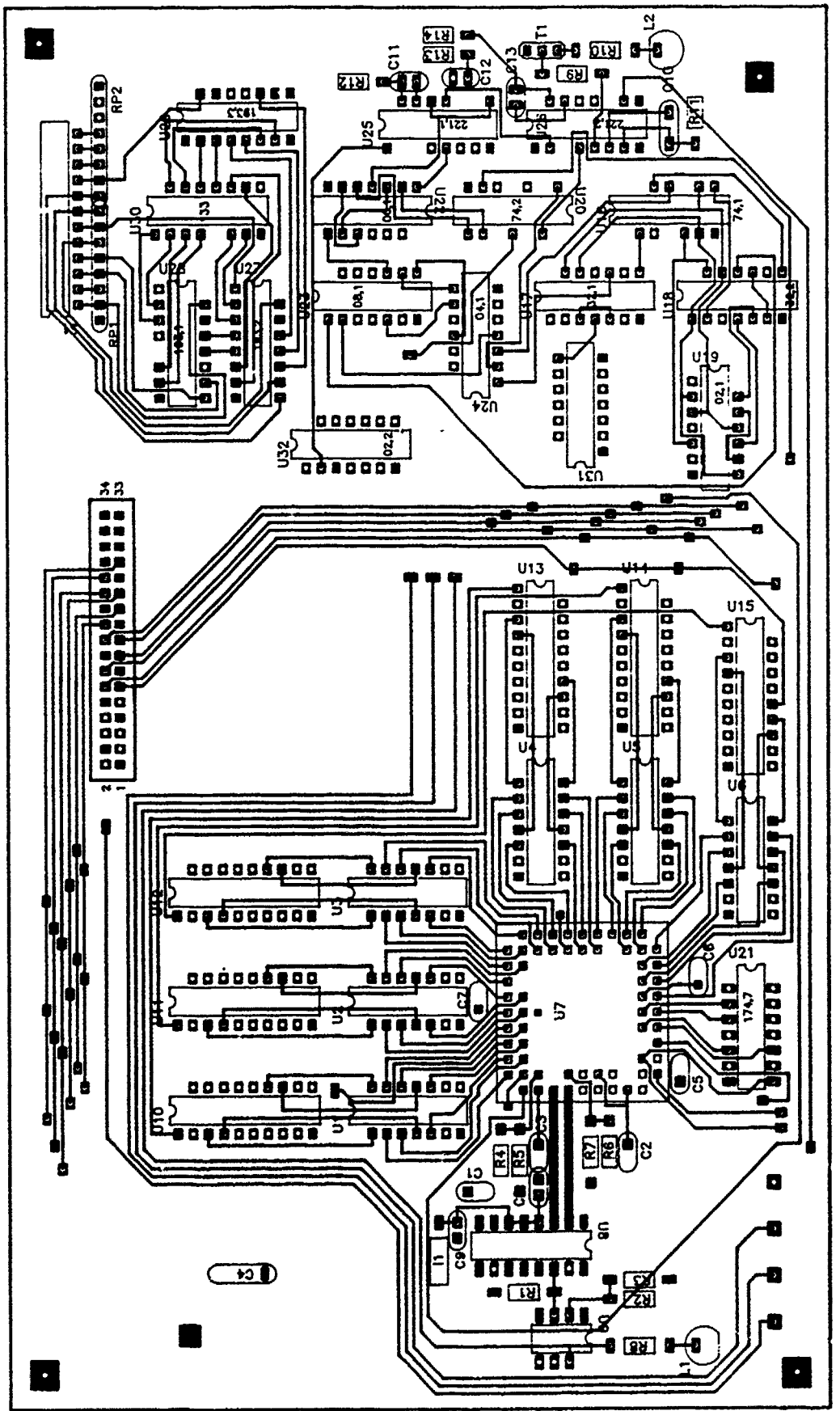


Figure 18. ITL Receiver Board - PC Board Layout (BOTTOM)

Bill of Materials ITL-RCVR.PCB

200MBIT/SEC ITL

Quantity	Type	Value	Ref Designators
11	.01uF	.01uF	C1,C2,C3,C5,C6,C7,C8,C9, C11,C12,C13
1	.1uH	.1uH	I1
1	1uF	1uF	C10
1	2.2K	2.2K	R9
1	2N3904	2N3904	T1
1	7.5K	7.5K	R14
2	10K	10K	R12,R13
1	10uF	10uF	C4
1	12 DIP SWITCH	12 DIP SWITCH	S1
1	20MHz	20MHz	U31
1	74HC00,1	74HC00,1	U22
1	74HC02	100K	U32
1	74HC02,1	74HC02,1	U19
1	74HC04,1	74HC04,1	U24
1	74HC08,1	74HC08,1	U23
1	74HC32,1	74HC32,1	U17
1	74HC32,2	74HC32,2	U18
1	74HC74,1	74HC74,1	U16
1	74HC74,2	74HC74,2	U20
1	74HC133,1	74HC133,1	U30
1	74HC174,1	74HC174,1	U1
1	74HC174,2	74HC174,2	U2
1	74HC174,3	74HC174,3	U3
1	74HC174,4	74HC174,4	U4
1	74HC174,5	74HC174,5	U5
1	74HC174,6	74HC174,6	U6
1	74HC174,7	74HC174,7	U21
1	74HC193,1	74HC193,1	U27
1	74HC193,2	74HC193,2	U28
1	74HC193,3	74HC193,3	U29
1	74HC221,1	74HC221,1	U25
1	74HC221,2	74HC221,2	U26
1	74HC374,1	74HC374,1	U10
1	74HC374,2	74HC374,2	U11
1	74HC374,3	74HC374,3	U12
1	74HC374,4	74HC374,4	U13
1	74HC374,5	74HC374,5	U14
1	74HC374,6	74HC374,6	U15
2	82ohm	82ohm	R4,R6
2	100K	100K	RP1,RP2
2	130ohm	130ohm	R5,R7
1	180ohm	180ohm	R10
1	220ohm	220ohm	R8
1	470K	470K	R11
1	1252N	AT&T 1252N	U8
1	GA9011	GA9011	U7
1	GRNLED	GRNLED	L1
1	LM311	LM311	U9
1	REDLED	REDLED	L2

Bill of Materials ITL-RCVR.PCB

200MBIT/SEC ITL

Quantity	Type	Value	Ref Designators
1	RES400	82ohm	R2
1	RES400	220ohm	R3
1	RES400	470ohm	R1

Appendix C. *Error Rate Test Circuit - Schematics*

1 of 3

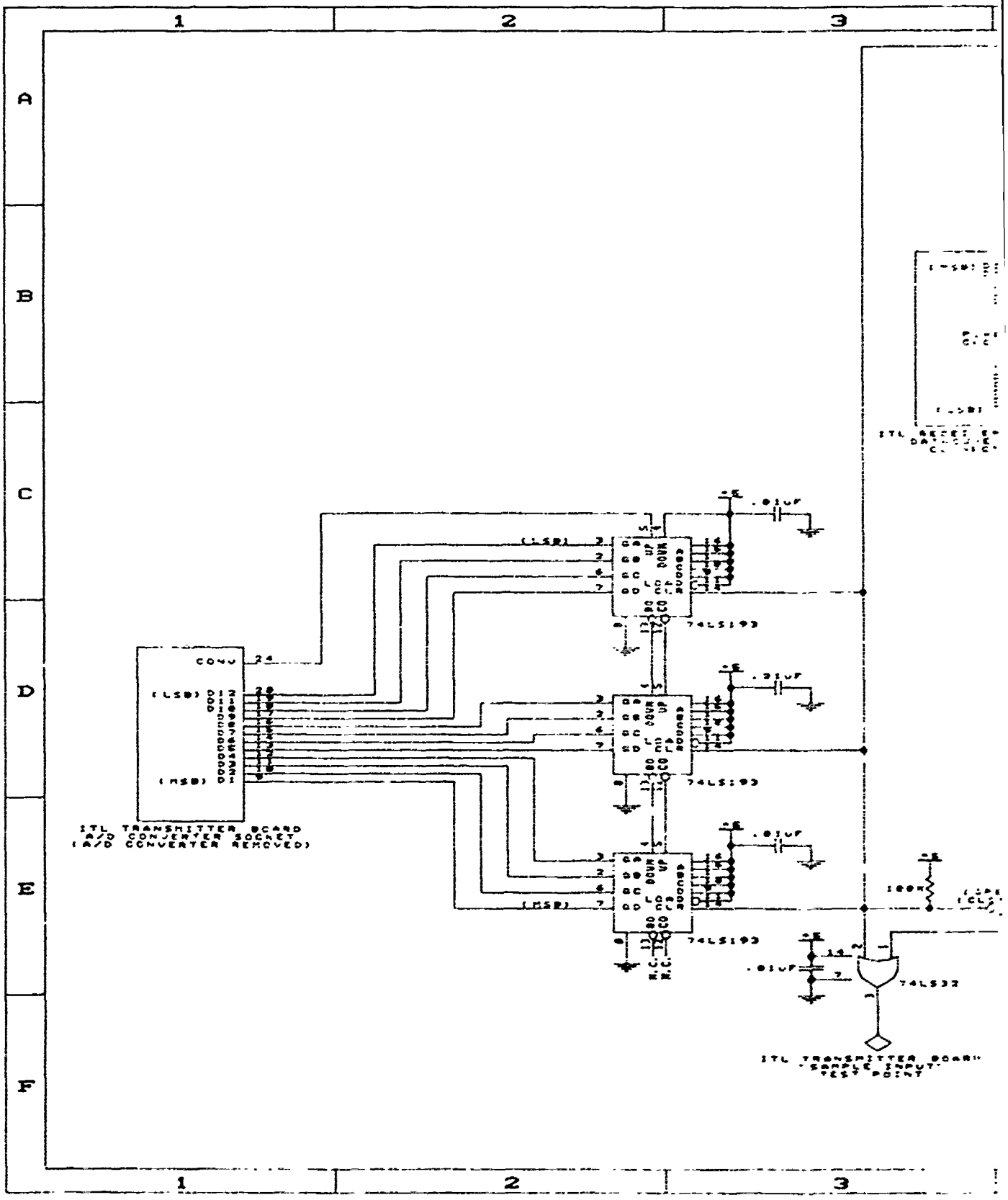
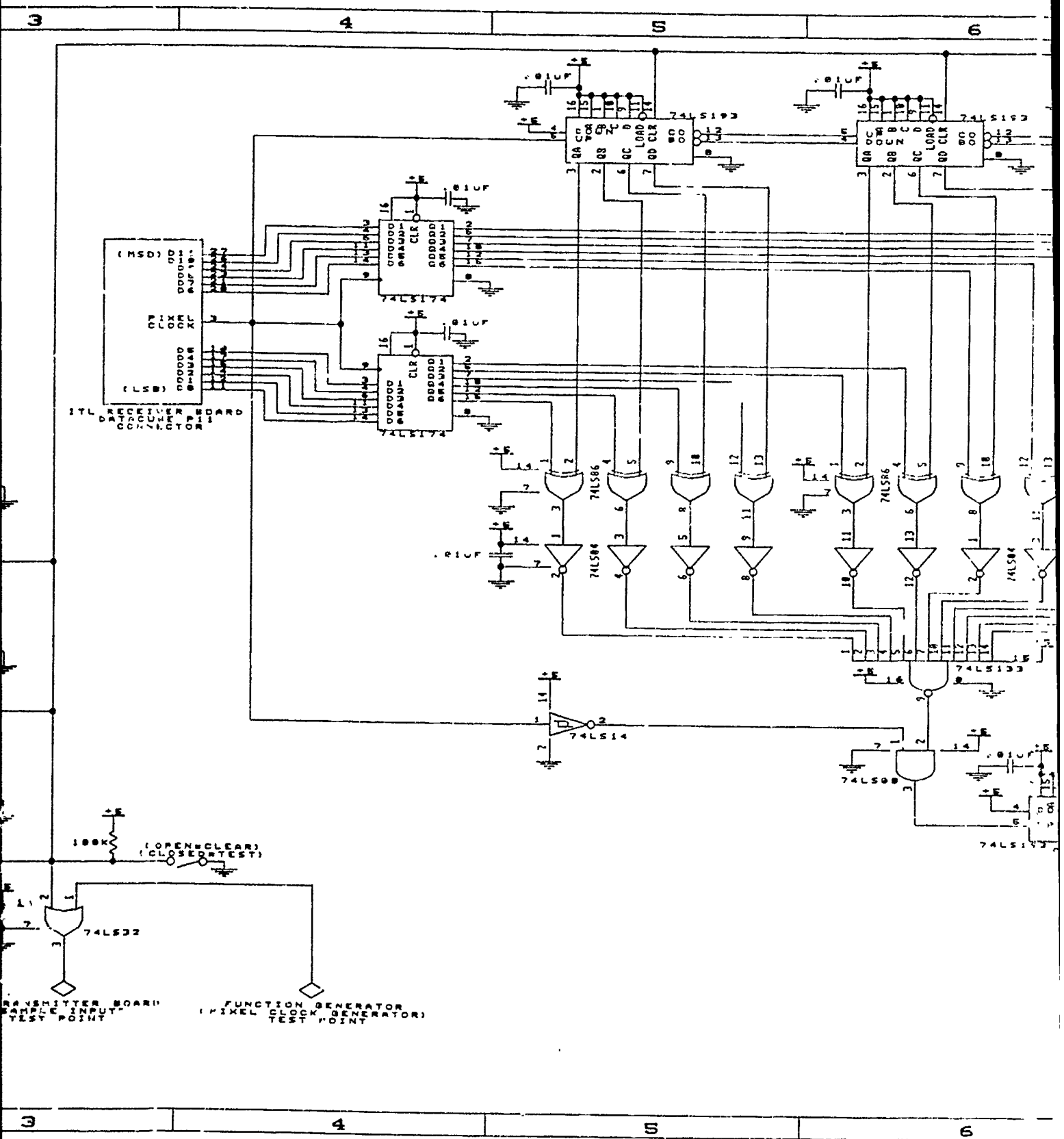
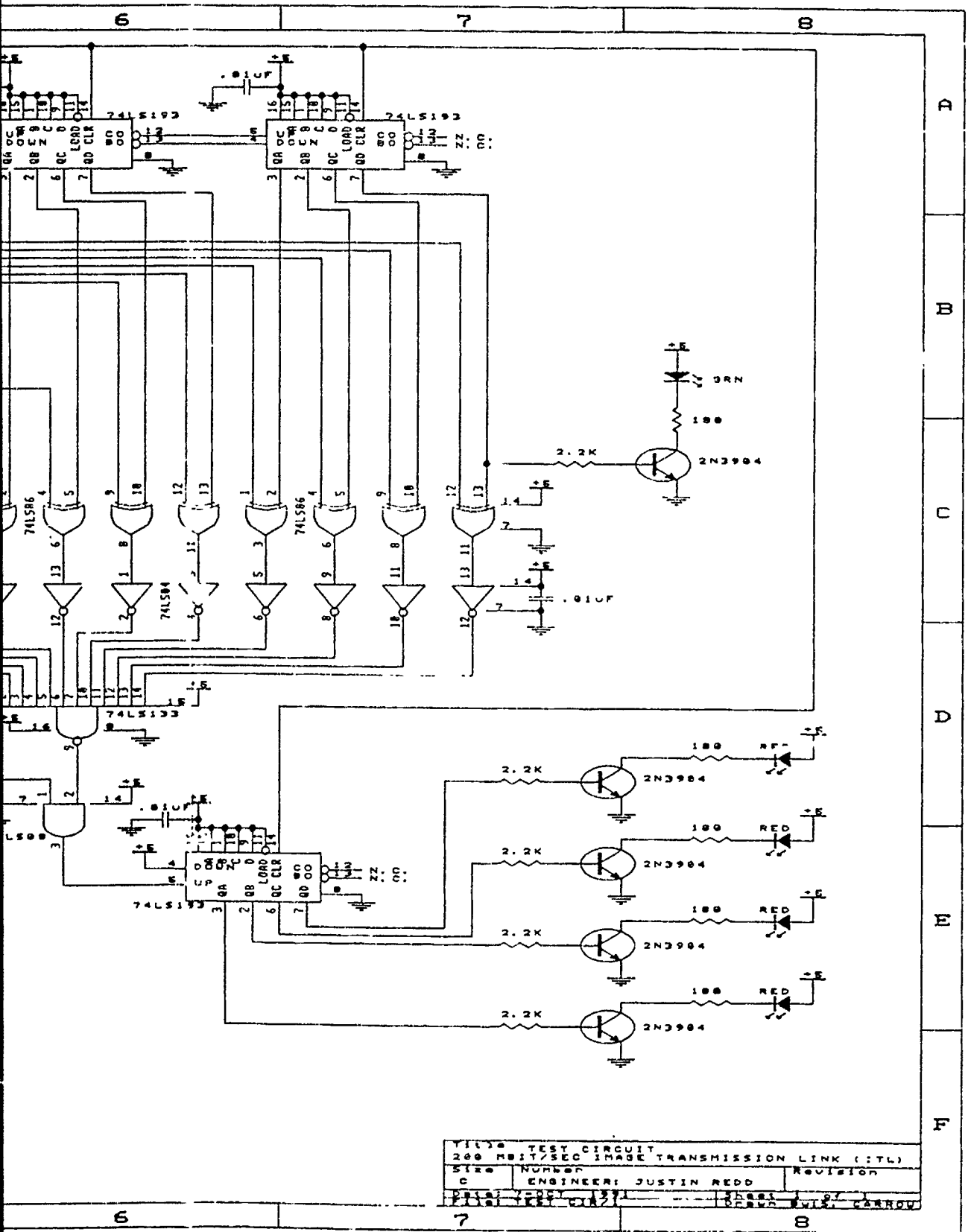


Figure 19. Error Rate Test Circuit - Schematics

2 of 3


3
4
5
6
74LS193
74LS174
74LS86
74LS04
74LS133
74LS14
74LS08
74LS32
100K
(OPEN=CLEAR)
(CLOSED=TEST)
ITL RECEIVER BOARD
(MSD)
(LSB)
PIXEL CLOCK
FUNCTION GENERATOR
(PIXEL CLOCK GENERATOR)
TEST POINT


6
7
8
A
B
C
D
E
F
74LS193
74LS86
74LS04
74LS133
74LS08
.01UF
2.2K
2N3904
GRN
100
RED
TEST CIRCUIT
200 MBIT/SEC IMAGE TRANSMISSION LINK (:TL)
Size
C
Number
Revision
ENGINEER: JUSTIN REDD

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